60299500

CONTROL DATA CORPORATION

INSTANT SMM REFERENCE MANUAL

CDC® COMPUTER SYSTEMS:
6000 SERIES
CYBER 70
CYBER 170

CONTROL DATA
CORPORATION

CONTROL DATA®
6000
CYBER 70
CYBER 170
COMPUTER SYSTEMS

INSTANT SMM
REFERENCE MANUAL

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PREFACE

This manual is a condensed version of CONTROL DATA® 6000/CYBER 70/CYBER 170 Reference Manual (publication no. 60160600) and 6000/CYBER 70/CYBER 170 Supplemental Reference Manual (publication no. 60409500). It does not replace either of these publications; it is to be used in conjunction with them.

This manual is intended for use by maintenance personnel performing preventive and emergency maintenance.

CONTENTS

DEADSTART PANEL SETTINGS

80-COLUMN ABSOLUTE BINARY CARDS

Address	Setting	
0001	75cc	Deactivate channel cc.
0002	77cc	
0003	e000	Connect card reader
0004	77cc	
0005	0001	Select binary read.
0006	77cc	
0007	1500	Select DCC to read.
0010	2000	
0011	7760	Load word count.
0012	74cc	Activate channel cc.
0013	71cc	
0014	0000 or 7773	Input address.
0015 †	XXXX	
0016 †	XXXX	
0017 †	XXXX	
0020 †	XXXX	

cc Card reader channel number (12 or 13)
e Card reader equipment number (4, 5, 6, or 7)
X Inconsequential

COMPASS BINARY DEADSTART CARDS

Address	Setting	
0001	75cc	Activate channel cc.
0002	77cc	
0003	e000	Connect card reader.
0004	77cc	
0005	0001	Select binary read.
0006	77cc	
0007	1400	Read one card.
0010	74cc	Activate channel.
0011	71cc	
0012	7666	Input address.
0013	XXXX	
0014	XXXX	
0015 †	XXXX	
0016 †	XXXX	
0017 †	XXXX	
0020 †	XXXX	

cc Card reader channel number (12 or 13)
e Card reader equipment number (4, 5, 6, or 7)
X Inconsequential

† CYBER 170 only.

60X/65X TAPE LOAD ON UNASSIGNED CHANNELS

The following panel setting is used for 60X/65X tape load on channel 12, 13, 32, or 33.

Address	Setting	
0001	75cc	Deactivate channel c.
0002	77cc	Connect tape drive.
0003	eruu	
0004	77cc	Rewind tape.
0005	0010	
0006	77cc	Read physical record.
0007	1400	
0010	74cc	Activate channel c.
0011	71cc	Input to address 0013.
0012	0013	
0013	XXXX	
0014	XXXX	
0015 †	XXXX	
0016 †	XXXX	
0017 †	XXXX	
0020 †	XXXX	

cc Tape channel number (12, 13, 32, or 33)
e Tape controller number (4, 5, 6, or 7)
uu Tape unit number
r Bypass CM if equal to 7 octal
X Inconsequential

60X/65X TAPE LOAD ON ASSIGNED CHANNELS

The following deadstart panel setting is used for 60X/65X tape load on channels 1 through 7 and 11 or 20 through 31.

Address	Setting	
0001	75cc	Deactivate channel c.
0002	77cc	Connect card reader e.
0003	e000	
0004	77cc	Set binary.
0005	0001	
0006	77cc	Read physical record.
0007	1400	
0010	74cc	Activate channel cc.
0011	71cc	Input to address 7666.
0012	7666	
0013	XXXX	

cc Tape channel number (12, 13, 32, or 33)
e Tape controller number (4, 5, 6, or 7)
X Inconsequential

† CYBER 170 only.

Address	Setting
0014	XXXX
0015 †	XXXX
0016 †	XXXX
0017 †	XXXX
0020 †	XXXX

This setting loads a card into PPU 0 at address 7666. The card is obtained by assembling and punching program PTL on the SMM program library.

66X WARMSTART ON UNASSIGNED CHANNELS

The following panel setting is used for warmstart of 66X on channel 12, 13, 32, or 33.

Address	Setting	
0001	75cc	Deactivate channel cc.
0002	1701	Delay.
0003	0576	
0004	2400 ††	Pass.
0005	24r0 ††	Pass.
0006	77cc	Connect and read tape unit u.
0007	ed6u	
0010	74cc	Activate channel cc.
0011	71cc	Input to address 0013.
0012	0013	
0013	XXXX	
0014	XXXX	
0015 †	XXXX	
0016 †	XXXX	
0017 †	XXXX	
0020 †	XXXX	

cc Tape channel number (12, 13, 32, or 33)
e Tape controller number (4, 5, 6, or 7)
u Tape unit number
r Bypass CM if equal to 7 octal
d 7-track tape density (0=556, 1=800)
X Inconsequential

† CYBER 170 only.
†† If a Data Channel Converter (DCC), a 6681, or a 6684 is on the channel, these instructions should be:

0004	77cc	Deselect DCC.
0005	2100	

66X WARMSTART ON ASSIGNED CHANNELS

The following deadstart panel setting is used for warmstart of 66X on channels 1 through 7, 11, and 20 through 31.

SMM is initialized by deadstarting a binary card deck obtained by assembling PT6 on the UPDATE I OLDPL tape.

Address	Setting	
0001	75cc	Deactivate channel cc.
0002	1701	Delay.
0003	0576	
0004	77cc	Connect card reader e.
0005	ertt	
0006	77cc	Read physical record.
0007	14dl	
0010	74cc	Activate channel cc.
0011	71cc	Input to address 7664.
0012	7664	
0013	00uu	
0014	XXXX	
0015 †	XXXX	
0016 †	XXXX	
0017 †	XXXX	
0020 †	XXXX	

cc Card reader channel number (12 or 13)
e Card reader equipment number (4,5,6, or 7)
uu Tape unit number
r CM bypass (7 octal)
d 7-track tape density (0=556, 1=800)
tt Magnetic tape system channel number
X Inconsequential

66X COLDSTART

The following deadstart panel setting is used for coldstart of a 66X/7021 Magnetic Tape System (MTS) on various channels. Coldstart accomplishes the load of the controlware into the MTS. Once the MTS has been coldstarted, the warmstart procedure (deadstart procedure that assumes the controlware has been loaded and is intact) should be followed.

†CYBER 170 only.

Card Reader on Channel 12 or 13		Card Reader on Channels 1 through 7 and 11	
Address	Setting	Address	Setting
0001	75cc	0001	73cc
0002	2400	0002	0013
0003	2400	0003	75cc
0004	77cc	0004	77cc
0005	ertt	0005	ertt
0006	77cc	0006	77cc
0007	14ds	0007	14ds
0010	74cc	0010	74cc
0011	71cc	0011	71cc
0012	7664	0012	7664
0013	00uu	0013	0000
0014	XXXX	0014	7112 †
0015 ††	XXXX	0015 ††	XXXX
0016 ††	XXXX	0016 ††	XXXX
0017 ††	XXXX	0017 ††	XXXX
0020 ††	XXXX	0020 ††	XXXX

cc Card reader channel number
e Card reader equipment number (4, 5, 6, or 7)
u Tape unit number (if card reader on channel 12 or 13)
s PPU0 save switch (1 if PPU0 will not be saved)
r CM bypass if 7 octal
d 7-track tape density (0=556, 1=800)
tt Magnetic tape system channel number
X Inconsequential

A deadstart SMM from MTS (66X) tape subsystem controlware deck must be available.

669/7152 MAGNETIC TAPE CONTROLLER COLDSTART ON UNASSIGNED CHANNELS

The following deadstart panel setting loads the 7152 Magnetic Tape Controller controlware from a 669 tape drive to the controller and starts the controlware executing. The controller must be on channel 0, 12, 13, 32, or 33. After coldstart has been accomplished, a warmstart can be used to deadstart the SMM system from an SMM tape.

† If MTS is on channel 12, change word 0014 to 7113.
†† CYBER 170 only.

Address	Setting	
0001	75cc†	Deactivate channel cc.
0002	1701	Delay loop.
0003	0576	
0004	2400††	Pass.
0005	2400††	Pass.
0006	77cc	Coldstart function; initiates the execution of the PROM program to load the controlware from the tape mounted on unit 1u.†††
0007	007u†††	
0010	0300	Halt; hangs the PP.
0011	XXXX	
0012	XXXX	
0013	XXXX	
0014	XXXX	
0015	XXXX	
0016	XXXX	
0017	XXXX	
0020	XXXX	

cc 7152 Magnetic Tape Controller channel (0, 12, 13, 32, or 33).
u Second octal digit of tape drive unit number.
X Inconsequential.

669/7152 MAGNETIC TAPE CONTROLLER COLDSTART ON ASSIGNED CHANNELS

The following deadstart panel setting loads the 7152 Magnetic Tape Controller controlware from a 669 tape drive to the controller and starts the controlware executing. The controller must be on channel 1 through 7, 11, or 20 through 31. After coldstart has been accomplished, a warmstart can be used to deadstart the SMM system from an SMM tape.

---

† If the channel cc, equals zero, this instruction must be 7540.

†† If a 6681, 6684, or CDC CYBER 170 data channel converter is on the channel, the instructions should be:

0004	77cc	Deselect data channel
0005	2100	converter.

††† Tape unit number must be in the range 10-17 octal. u is the second octal digit of the unit number.

Address	Setting	
0001	1402	Output halt program to the PP assigned to channel cc.
0002	73cc	
0003	0013	
0004	75cc	Deactivate channel cc.
0005	1701	Delay loop.
0006	0576	
0007	2400†	Pass.
0010	2400†	Pass.
0011	77cc	Coldstart function, initiates the execution of the PROM program to load the controlware from the tape mounted on unit 1u. ††
0012	007u	
0013	0000	Halt program for PP assigned to channel cc.
0014	0300	
0015	XXXX	
0016	XXXX	
0017	XXXX	
0020	XXXX	

cc 7152 Magnetic Tape Controller channel (1-7, 11, or 20-31).

u Second octal digit of tape drive unit number.

X Inconsequential.

844/7152 DISK CONTROLLER COLDSTART ON UNASSIGNED CHANNELS

The following deadstart panel setting loads the 7152/844 Disk Controller controlware from a prerecorded 844 disk pack mounted on unit uu and starts the controlware executing. The controller must be on channel 0, 12, 13, 32, or 33. After coldstart has been accomplished, a warmstart can be used to deadstart the SMM system from the disk. †††

†If a 6681, 6684, or CDC CYBER 170 data channel converter is on the channel, the instructions should be:

0004	77cc	Deselect data channel
0005	2100	converter.

††Tape unit number must be in the range 10-17 octal. u is the second octal digit of the unit number.

†††Refer to LDC utility for a discussion of how the controlware is written onto an 844 disk pack. For a discussion of how the deadstart sector program and the SMM systems are loaded to an 844 disk pack, refer to TD1 utility in publication number 60160600.

Address	Setting	
0001	75cc†	Deactivate channel cc.
0002	77cc	Function controller to
0003	01uu	coldstart using disk unit uu.
0004	0300	Halt; hangs the PP.
0005	XXXX	
0006	XXXX	
0007	XXXX	
0010	XXXX	
0011	XXXX	
0012	XXXX	
0013	XXXX	
0014	XXXX	
0015	XXXX	
0016	XXXX	
0017	XXXX	
0020	XXXX	

cc 7152/844 Disk Controller channel (0, 12, 13, 32, or 33).

uu 844 disk drive unit number (00-03) with prerecorded controlware disk pack.

X Inconsequential.

844/7152 DISK CONTROLLER COLDSTART ON ASSIGNED CHANNELS

The following deadstart panel setting loads the 7152/844 Disk Controller controlware from a prerecorded 844 disk pack mounted on unit uu and starts the controlware executing. The controller must be on channel 1 through 7, 11, or 20 through 31. After coldstart has been accomplished, a warmstart can be used to deadstart the SMM system from the disk.††

† If the channel cc equals zero, this instruction must be 7540.

†† Refer to LDC utility for a discussion of how the controlware is written onto an 844 disk pack. For a discussion of how the deadstart sector program and the SMM system are loaded to an 844 disk pack, refer to TDI utility in publication number 60160600.

Address	Setting	
0001	1402	Output halt program to
0002	73cc	the PP assigned to chan-
0003	0007	nel cc.
0004	75cc	Deactivate channel cc.
0005	77cc	Send function to control-
0006	01uu	ler to coldstart using disk unit uu.
0007	0000	Halt program for PP
0010	0300	assigned to channel cc.
0011	XXXX	
0012	XXXX	
0013	XXXX	
0014	XXXX	
0015	XXXX	
0016	XXXX	
0017	XXXX	
0020	XXXX	

cc 7152/844 Disk Controller channel (1-7, 11, or 20-31).

uu 844 disk drive unit number (00-03) with prerecorded controlware disk pack.

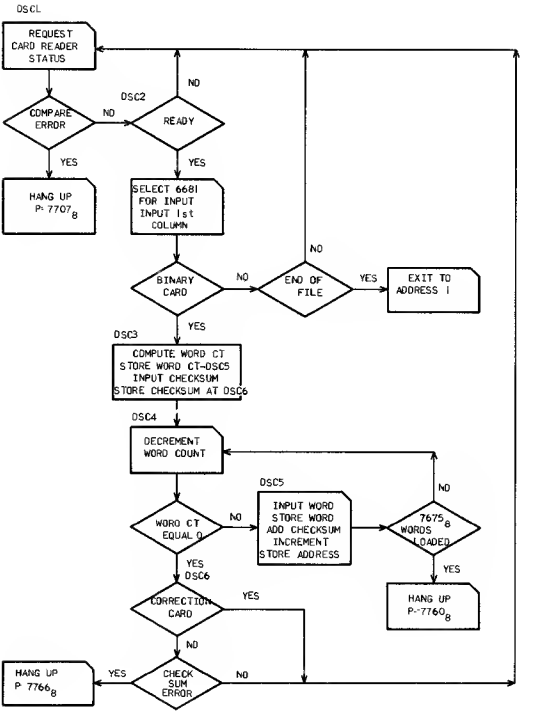
X Inconsequential.

CEJ/MEJ SWITCH SETTINGS

The following tests require the CEJ/MEJ switch settings to run properly. All other tests can run with the CEJ/MEJ switch in either position without affecting the operation of the test.

CEJ/MEJ ENABLED	CEJ/MEJ DISABLED
CNF	CPM
CPX	CT1
IAS	EJ1
MAN	ERX
MXJ	EJT

DEADSTART CARD LOADER (DSCL)



PERIPHERAL PROCESSOR DEADSTART COMMAND TEST (CED)

CED is an in-line, fixed-operand, sequential command and memory retention test that executes in PPU 0 following deadstart. It verifies basic operands and instructions in PPU 0 before the execution of the preload display program CEL. A two-PRU version is used in the field, and a one-PRU version is used for manufacturing.

CED executes on any 6000/CYBER 70/CYBER 170 configuration, PPU 0, channel 0, magnetic tape equipment (60X/65X/66X), and channel.

CED DEADSTART PANEL SETTINGS

CED is loaded by the standard deadstart panel setting or by an alternate panel setting for the one-PRU version. This program is reentered at address 6 to load the second segment (or PRU 2 of the two-PRU version only) and the preloader display CEL.

Abbreviations for the following table are as follows:

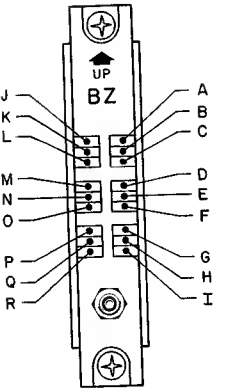
C = Magnetic tape channel number
U = Magnetic tape unit number
E = Magnetic tape equipment number
Y = Disk channel number
V = Disk unit number
F = Disk equipment number
W = Starting address to load SMM from disk
A = 0 for CYBER 17X, 1 for 6X00, and 2 for CYBER 7X
B = 6 for CYBER 17X and N for 6X00/CYBER 7X (refer to publication no. 60160600 for N)
X = Not used
* = CYBER 17X only
\+ = 24CC and 24RS if no DCC/6681 is on channel C
D = Density, 0=556 and 2=800 [refer to MTS (66X) ERS]
R, S, Z = Refer to publication no. 60160600, CED description

	60X/65X	66X	66X after CED Executes	60X/65X One-PRU CED	60X/65X after One-PRU CED Executes	66X One-PRU CED	66X after One-PRU CED Executes	Display Contents of Memory at H33
01	75CC	75CC	75CC	75CC	75CC	75CC	75CC	4007
02	77CC	1701	77CC	77CC	77CC	1701	77CC+	3507
03	ERUU	0576	21RS	ERUU	ERUU	0576	21RS+	2000
04	77CC	77CC	77CC	77CC	77CC	77CC+	77CC	0300
05	ZZ10	21RS	E02U	ZZ10	ZZ10	21RS+	E02U	4407
06	77CC	77CC	77CC	77CC	77CC	77CC	77CC	0100
07	140S	ED6U	E04U	140S	140S	ED6U	E04U	ADDR
10	74CC	74CC	74CC	74CC	74CC	74CC	74CC	XXXX
11	71CC	71CC	71CC	71CC	71CC	71CC	71CC	XXXX
12	0013	0013	0013	0021	0021	0021	0021	XXXX
13	XXXX	XXXX	XXXX	03AB	WWWN	03AB	WWWN	XXXX
14	XXXX	XXXX	XXXX	YYVF	YYVF	YYVF	YYVF	XXXX
15 †	XXXX	XXXX	XXXX	WWWN	WWWN	WWWN	WWWN	XXXX
16 †	XXXX	XXXX	XXXX	XXXX	03AB	XXXX	03AB	XXXX
17 †	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
20 †	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX

PPS CHASSIS BIT LIGHTS (CYBER 17X ONLY)

No messages are displayed. Detection of an error executes a 0300, 0400, 0500, 0600, or 0700 instruction to stop the PPU. The address of the failing instruction sequence may be read from the SCR P register lights at H33 on CYBER 170 or by scoping the PPU 0 address register at C01 and C02 on the 6000/CYBER 70.

Location	Bit No. (Decimal)	Bit No. (Octal)	Description
F39-A	084	124	2X speed
F39-B	085	125	Inhibit CMC required
F39-C	086	126	Not used
F39-D	087	127	Not used
F39-E	088	130	CEL loaded
F39-F	089	131	Memory test OK
F39-G	090	132	Compare test OK
F39-H	091	133	Second PRU loaded
F39-I	092	134	Instruction test OK
F39-J	093	135	Not used
F39-K	094	136	Not used
F39-L	095	137	Stop on PP memory PE
F39-M	192	300	CP-0 stopped
F39-N	193	301	CP-1 stopped
F39-O	194	302	ECS in progress flag
F39-P	195	303	Monitor flag CP-0
F39-Q	196	304	Monitor flag CP-1
F39-R	197	305	Not used
H33-A	060	074	PPS P register bit 0
H33-B	061	075	PPS P register bit 1
H33-C	062	076	PPS P register bit 2
H33-D	063	077	PPS P register bit 3
H33-E	064	100	PPS P register bit 4
H33-F	065	101	PPS P register bit 5
H33-G	066	102	PPS P register bit 6
H33-H	067	103	PPS P register bit 7
H33-I	068	104	PPS P register bit 8
H33-J	069	105	PPS P register bit 9
H33-K	070	106	PPS P register bit 10
H33-L	071	107	PPS P register bit 11
H33-M	072	110	PP code bit 0
H33-N	073	111	PP code bit 1
H33-O	074	112	PP code bit 2
H33-P	075	113	PP code bit 3
H33-Q	076	114	PPS breakpoint bit
H33-R	077	115	CMC breakpoint bit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I

PRELOAD CONTROL PROGRAM (CEL)

Following the successful execution of the deadstart diagnostic CEQ, CEL is loaded and initiated. The function of CEL is to interpret keyboard input directives describing a parameter change or requesting the loading and initiating of a PPU 0 program, a system utility program, or the SMM system. The following is a list of these directives.

†SYbb,IIII (cr)	Change the configuration for 6000 and CYBER 70 description, where bb = number of banks and IIII = CPU type. Example: SY40, 7428.
SYbbb,III,c,pp (cr) or SYbb,III,c,pp (cr)	Change of configuration description for CYBER 170. bbb = Number of banks III = CPU type C = Number CPU (1 or 2) pp = Number of PPUs Example: SY100, 175, 1, 20 or SY40, 175 2, 10.
xxWyyyy(cr)	Change the contents of address xx of the deadstart area (1 through 14B0) to yyyy (for 6000/CYBER 70).
xxWyyyy (cr)	Change the contents of address (xx) of the deadstart area (1 through 20B) to yyyy on CYBER 170 machines only.
xx+yyyy (cr)	Similar to the previous entry, except 1 is added to xx allowing sequential entry.
yyyy (cr)	Status/control register functions. (Refer to CYBER 17X Reference Manual.) This command will execute the status/control register function, where yyyy is the octal function code.

† The configuration and mass storage device parameters are saved in CM addresses 1 and 242, respectively, when SMM is initiated so successive deadstarts will not require defining these parameters. If this feature is not desired, set 03 = E7UU to eliminate this use of CM.

†CR	Loads and initiates the program selected by the contents of addresses 13 and 14. This is typically used on successive deadstarts following a preload of mass storage (PX).
MNE (cr)	Direct loads and initiates PPU 0 program MNE without using CM.
T (cr)	Loads and initiates the SMM system using the deadstart tape as the library media.
† PX (cr)	Loads and initiates the utility tape to mass storage program TD1 using device type X. (The starting position, device channel, and equipment are assumed to be contained in addresses 13 and 14 on the right screen display.) X=1-808, 2-6603/844, 3-81X/821, 4-85X/841, 5-86X. If X is absent, the device type described in address 13 is used. Refer to TD1 writeup for 13 and 14 parameters.
D (cr)	Loads and initiates the utility dump program DDD.
R (cr)	Redeadstart by returning PPUs to deadstart condition and execute the deadstart program displayed beginning with address 2. (A use of this feature is to deadstart from a different tape unit without changing the deadstart panel. Set 03W EOUU and then R cr.)
CP (cr)	Clears all PPU memories to zero, except PP0.

† The configuration and mass storage device parameters are saved in CM addresses 1 and 242, respectively, when SMM is initiated so successive deadstarts will not require redefining these parameters. If this feature is not desired, set 03 = E7UU to eliminate this use of CM.

CC (cr)	Clears all central memory to zero.
* (cr)	Sets all PPUs to 2X speed (CYBER 170 only).
= (cr)	Toggle right screen display selection (deadstart area or status control words).

Site parameters describing system configuration (SYbb, IIII) and mass storage starting position, channel, unit, and equipment (DS13 and DS14) may be permanently edited onto the deadstart tape using edit routines EDT (SMM) or EDIT (SCOPE).

MEMORY DUMP ROUTINE (DDD)

)DD is called by using the CEL loader and typing D.
)DD will be loaded and display the following messages.

P, C, X, I, F, T, A

P — This selection allows the operator to dump any PP to the printer.

LP CH	(Type in channel number)
LP NO	(Type in equipment number)

C — This selection allows the operator to dump central memory to the printer.

CM from	(Type in starting CM address to be dumped)
CM to	(Type in last CM address to be dumped)

X — This selection allows the operator to exchange out CP0 or CP1 and dump the exchange package to the printer.

I — This selection is used only to fill the 512 image.

F — This selection is used only to fill the 580 image.

T — This selection allows the operator to dump central memory to tape 1 or load one file from tape 1 into central memory. (Number of banks selected must be in octal.)

A — This selection is used only to fill the 580 PFC memory.

All information required for any of these options is displayed on the 6000 console.

DDD resides in PPU-0 in low core starting at location 22B. If PPU-0 is dumped, low core has been clobbered by DDD. If low core must be saved, transfer PPU-0 memory to another PPU before loading DDD.

Example: To dump PPU-0 to PPU-1, set deadstart panel to:

```
0001    2001
0002    0000
0003    7301
0004    0000
0005    0300
```

Then deadstart to transfer PPU-0 to PPU-1.

Reset the deadstart panel to load DDD and dump PPU-1.

DDD contains the option to add multiple access controllers if site configuration requires. The following example activates this option when assembled during a correct or update run of DDD.

```
*IDENT XXXX
*I DDD.15
DF.1015    EQU      1
*C DDD
```

TAPE TO DISK (TD1)

TD1 is a utility routine that loads the SMM library from the SMM tape to a disk. An option permits TD1 to load an 844 disk with a deadstart sector program that permits a direct deadstart from the disk.

OPERATIONAL PROCEDURE

RESTRICTIONS

1. The disk cannot be connected to the same channel as the tape controller.
2. Central memory must contain a disk directory.
3. Controlware MA710-A09 or above must be installed to write a disk deadstart sector program to an 844 disk.

LOADING PROCEDURE

The following steps load the SMM library onto the disk. This procedure is used to run SMM for maintenance.

1. Deadstart using panel settings for tape load of SMM.
2. Load TD1 by typing:

   Px (cr)

   x = equipment type (refer to Parameters). CEL option word 13 indicates the beginning address where SMM will be written to the disk.
3. Press any key except X to dump SMM tape to disk. When dump is complete, a message appears indicating where SMM resides (refer to Normal Messages).

   To load the disk deadstart sector program to an 844 disk, continue to step 4.
4. Deadstart again using same panel settings as step 1.
5. Type P2 (cr) to load TD1.

NOTE

CEL option word 13 must be identical for steps 2 and 5 so that the deadstart sector program can locate the SMM library.

6. Press X key to load deadstart sector program to 844 disk. A deadstart panel display appears on screen.
7. Set deadstart panel to conform to display appearing in step 6.
8. To deadstart from disk, press the DEADSTART switch. CPC display appears. Successive deadstarts do not require reloading the sector.

PARAMETERS

Word 13 = ZZZX

ZZZ = Starting disk address to load SMM (cyl + pos)

X = 1 for 808
2 for 6603/844
3 for 813/814/824
4 for 853/854/841
5 for 861/863/865

Word 14 = YYUE

YY = Channel number of the disk
U = Unit number of the disk
E = Equipment number of the disk

NORMAL MESSAGES

The following deadstart panel setting messages appear on the left screen after the deadstart sector program has been written to the disk.

DEAD START PANEL SETTINGS
FOR 844 DISK DEAD START

FOR CHANNELS 0, 12, 13, 32, 33	ALL OTHER CHANNELS
1 = 75CC	1 = 1403
2 = 77CC	2 = 73CC
3 = 03UU	3 = 0012
4 = 74CC	4 = 75CC
5 = 71CC	5 = 77CC
6 = 0010	6 = 03UU
7 = 0303	7 = 74CC
	10 = 71CC
	11 = 0010
	12 = 0000
	13 = 7112
	14 = 0000

NOTE

If CC=0 set location 1 to 7540.

CC = Channel number
UU = Unit number

SMM INITIALIZATION

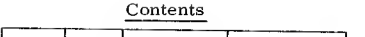
SMM consists of a loader/monitor program (LDR), a central processor control program (CPC), a central memory resident, and a collection of programs. This section considers the SMM elements LDR, CPC, central memory, and DDD.

1. LDR loads and enters its initialization routine.
   a. Tape channel, equipment, and unit numbers are read from deadstart settings and plugged into I/O instructions.
   b. The test list is written in the upper 200 CM words.
   c. CM addresses 0 through 400 are cleared.
   d. Tape parameters are written to CM address 241 and the loading device parameters are inserted in address 242.
   e. Number of PPUs are determined. Drop is written to PPU input registers that are not available.
   f. Computer type number of memory banks, number of CPUs, and number of PPUs are written into CM address 1.
   g. CPMTR is read from the SMM library to central memory, starting at address 250.
   h. CPC is read from SMM device and loaded into PPU 8.
   i. LDR exits to its monitor loop.
2. CPC enters its initialization routine.
   a. Computer type and number of memory banks are set in the left screen display.
   b. Field length and relative address are determined and set in exchange areas. Error mode is set for 7000 if the system is a CYBER 17X. Error exit selected on parity errors is a normal mode of operation for 17X systems.
   c. If two CPUs were indicated by LDR in CM address 1, a flag is set, which controls CPU P register display, CPU control, and memory display.
   d. Upon recognizing a stand alone, cr will go to multiprogramming mode of operation. For CYBER 170, a status control register monitor (MTR) will be loaded to PPU 1.
   e. CPC exits to its main loop.

CENTRAL MEMORY

SMM uses the following central memory locations.

Address	Contents
0	Zero
1	59 47 35 23 11 0 BKS | SYS | TYPE | CPU | PPU BKS — Number of 4K CM banks (OCT) SYS TYPE — Type of system in display code CPU — Number of CPUs -1 PPU — Number of PPUs
2	53 35 29 11 0 FL | RA | CPU This is set by CPC/EXC/MAN/etc. and used by LDR when loading programs.
3	02000 00003 Loop CPU instruction.
4	Name of last CPU 0 program loaded.
5	59 47 35 23 11 0 PP Num | Accept | Address | Bits | J display pointer.
6	Name of last CPU 1 program loaded.
7	EXC | EXCRA | | DMP DMP running flag. Nonzero when DMP is running. EXC loading flag. Nonzero when EXC is loading a CPU test. EXCRA = RA of CPU 0 EXC.

Address	Contents
10	

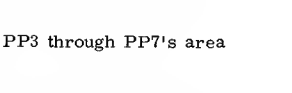
PP1 IR, Zero if PP is idle.

NME = Test name
CZ = Loading channel, cleared after test is loaded, then:
Z = Go/stop flag (1=go, 2=stop)
X = Abort flag (1=abort)
PARMS, if ≠ 0, are stored in MCP+2

11	

PP1 output register used to send functions to LDR and MTR

12 through 17	PP1's message buffer
20 through 27	PP2's area
30 through 77	PP3 through PP7's area

100	
101	
102	

PP8/10 (CPC) IR

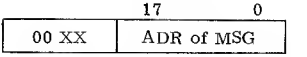
Output register
(byte 2=PP* if X. LP1, etc.)

AUTO=0 when auto mode
EXC≠0 when EXC, MAN, or BD1 is running

103 through 106	Message buffer

Address	Contents

107



DMP/CPU communication word

XX = 2 = CPU message
XX = 10 = dump dayfile to LP

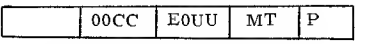
110 through 237 PP9/11 through PP19/31 area

240

Display control word

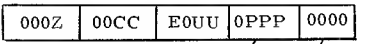
PP = PP that has the display

241



Magnetic tape parms, set by LDR

242



SMM device parms, set by LDR

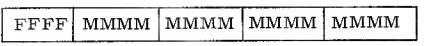
Z = Device code

First sector

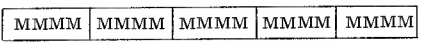
First position/cylinder

243 Counter for number of times CPMTR is entered

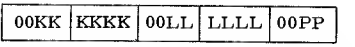
244



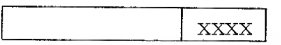
245



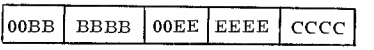
F = Function code to MTR
M = Message buffer to MTR

Address	Contents
246	

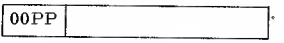
K = Starting address of K display
L = Starting address of L display
P = PPU in which MTR is loaded

250 through 274	Location of CPMTR program
275	

XXX ≠ 0 error CEJ occurred
Bit 4 = 1 signifies CPU 1
= 0 signifies CPU 0

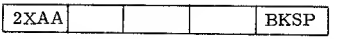
276	Location of CPMTR program
277	

B = Breakpoint for SIM
E = Input exchange package address
C = SIM/CPC control word

300 through 313	

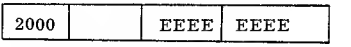
Channel status table for channels 0 through 13
PP = PPU number using channel, zero if not used

315	Error CEJ occurred flag
316	CPMTR control word for CPU 0
317	CPMTR control word for CPU 1
320 through 333	Same as 300 through 313 for second set of PPUs

Address	Contents
334	

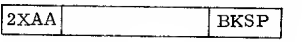
AA = Quantity added to exchange address to locate output exchange package after error CEJ

BKSP = No loop CEJ error if zero
Loop CEJ error if one

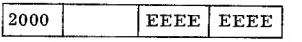
335 

2000 = SMM did not exchange if 0 SMM exchanged in

E = CPU 0 exchange package address

336 

Same as 334, except for CPU 1

337 

Same as 335, except for CPU 1

340	Address of CPU 0 monitor exchange address
360	Address of CPU 1 monitor exchange address
400 through 577	CPU 0 exchange package area
600 through 777	CPU 1 exchange package area
1000 through 10777	Overlay area for PPU 1
11000 through 20777	Overlay area for PPU 2
21000 through 101777	Other PPU overlay areas in order

Address	Contents
61000	Beginning address of CPC overlay
†XX5777	DMP recovery pointers
†XX6000 through XX6777	DMP I display buffer
†XX7200 through XX7237	40-word buffer for ECS reads
†XX7270 through XX7275	6-word message buffer CPC to DMP
†XX7300 through XX7347	Buffer area for J display
†XX7400 through XX7600	Buffer area for H display
†XX7601 through XX7776	Message instructions for H display

†XX is determined from memory size to put information in uppermost core.

REAL-TIME DISPLAY AND TIMING CLOCK FOR 6000 SMM (CLK)

PURPOSE

The intent of this routine is to provide a digital clock that may be sampled in order to compute run times of diagnostic software and related hardware operations. It can also be used as a source for a console display of the current real time.

REQUIREMENTS

HARDWARE

1. One 6000 PPU.
2. One 6000 real-time channel clock with a 4.096-millisecond period.
3. Equipment required by 6000 SMM to load any diagnostic.

SOFTWARE

This program will execute under SMM 6000's multi-processing scheme (that is, MLP or auto).

OPERATIONAL PROCEDURE

LOADING PROCEDURE

The program is called as CLK under the 6000 SMM system called auto. (Refer to SMM systems.)

PARAMETERS

There are no parameters. If a T is typed under the PPU display, the following message is displayed.

TIME. 00.00.00.

The desired time can then be entered. A backspace will cause the last digit entered to be zeroed out. A carriage return enters the desired value into the clock.

SECTION DESCRIPTION INDEX

Not applicable.

OPERATOR COMMUNICATION

MESSAGE FORMATS

Under the auto G display the message format is:

```
11 CLK  *00.00.00.
```

- 11 — PPU number that CLK is running into.
- * — Blank if the time has been set by the operator or * to indicate the time since CLK was loaded.

In the PPU registers in central memory (PPIR = PPU number *100B) under the E display:

CM Location	1	2	3	4	5	Display Code Values
PPIR+0	0314	1300	0000	0000	0000	CLK
PPIR+1	0000	0000	0000	0000	0000	
PPIR+2	4733	3357	3333	5733	3357	*00.00.00.
PPIR+3	ZERO	SCND	MLSC	MCSC	CHCK	ABCDEFGH
PPIR+4	CLPH	MSC1	MSC2	0000	0000	IJKLMN
PPIR+5	0000	0000	0000	0000	0000	
PPIR+6	0000	0000	0000	0000	0000	
PPIR+7	0000	0000	0000	0000	0000	

- PPIR — CLK's PPU number *100B.
- ZERO — Data zero which terminates the display clock message when displayed by SMM.
- SCND — A 12-bit octal-second counter (SEC).
- MLSC — A 12-bit octal-millisecond counter which is reset to zero when it reaches 1750B (that is, 1750B milliseconds = 1000 milliseconds = 1 second) (MSC).
- MCSC — A 12-bit octal-microsecond counter which indicates the time in microseconds, since the clock was last sampled (USC).
- CHCK — The current value of the channel 14B real-time clock.
- CLPH — The current phase of the real-time clock that CLK is writing to indicate that 1 millisecond has passed.
- MSC1 — Upper 12 bits of a 24-bit millisecond counter.
- MSC2 — Lower 12 bits of a 24-bit millisecond counter.

The previous information should be helpful to a programmer wishing to time an operation without requiring a PPU to go into a timing loop. Such loops can cause a communication gap that may be undesirable under system operations.

DESCRIPTION

This routine samples the clock about once every 45 microseconds. At each sample, a check is made to see if the clock's phase has changed (that is, the upper two bits of the real-time clock). When the clock phase changes, a millisecond has elapsed and all millisecond counters are updated. After 1000 milliseconds have elapsed, the second counter is incremented. This same procedure is used for minutes and hours. After 24 hours the clock returns to zero. A more detailed description may be obtained by studying the listing.

CENTRAL MEMORY CONFLICT PROGRAM (CMC)

OPERATIONAL PROCEDURE

RESTRICTIONS

1. This program should be run under the SMM auto mode of operation, along with EXC or individual CPU or CM tests or the SCOPE system.
2. No RA value is added to the CM address specified in the keyboard entry (under SMM). Refer to parameters for RA under SCOPE operation.

LOADING PROCEDURE

1. Called as X.CMC. or X.CMC,WWWZ. When called X.CMC., the program stops so that parameters may be entered. When called X.CMC,WWWZ., WWW x 10_8 is the delay count. If WWW is zero, a delay count of five is assumed. Z values have the following significance.

Z	= 0	Stop for parameters
	= 1	Read only
	= 2	Stop on error (always selected)
	= 3	Write only
	= 4	Read/write
	= 5	Write/read/compare

   CMC runs in central memory at an address equal to the PP number times 10000B. Refer to SCOPE Operation for on-line loading parameters.
2. May be called into as many PPUs as the system allows (under auto).

PARAMETERS AND/OR ENTRIES

Location 1500 = 0 - Do not stop on compare errors
= 2 - Stop on compare errors
= Sense switch 1 for SCOPE operation

Entries

The left screen displays entries (under SMM).

D	Release display to SMM system.
S	Stop read/write.
SPACE	Continue read/write.
(CR)	Restart and display entries.
T, X.	Set delay between reads/writes = X (1-7777). Preset to 1.
R, X, Y.	Read X(1-1000) words from central memory location Y into PP buffer at location 3000.
W, X, Y.	Write X(1-1000) words to central memory location Y from PP buffer at location 3000.
RW, X, Y.	Read X (1 through 1000) words from central memory location into PP at location 3000 and write X words to central memory location Y from PP location 3000.
WR, X, Y.	Write X (1 through 400) words from PP location 5400 to central memory location Y and read X words to PP location 3000 from central memory location Y, then compare data read to data written and display any compare errors.

SCOPE Operation

Load call = X. CMC, ABNNNN, FFFFFF.

Parameters for A, B, N, and F.

A = 1 through 7 to set time between reads and writes

	(octal)	(binary)
B =	0	(X00) - Read only
	1	(X01) - Write only
	2	(X10) - Read/write no compare
	3	(X11) - Write/read with compare
	4	(1XX) - Add RA to F and request FL from system

N = Number of words to read or write

F = Central memory address to read or write (refer to B for RA parameters)

MESSAGES

NORMAL

READING CM	Read CM only.
WRITING CM	Write CM only.
READ/WRITE CM	Read, write, and no compare.
WRITE/READ/COMPARE CM	Write, read, and compare data for errors.
MAKE ENTRY TO READ/WRITE CM	Assign display and make desired entries.

ERROR

EXP - VVVVWWWWXXXXYYYYZZZZ
REC - VVVVWWWWXXXXYYYYZZZZ
COMPARE ERR ADDR CCCCC

C = CM address where compare error occurred.
V-Z = The data expected (EXP) and the data received (REC-failing data).

NOTE

Data is compared one 12-bit word at a time until five (12-bit) words have been checked. Only those 12-bit words that actually do not compare are displayed as numbers. The 12-bit words that do compare are displayed as V, W, X, Y, or Z, depending upon the byte.

Under SMM, locations 0 through 1000 are protected on a write central memory. Illegal entries are ignored.

CENTRAL PROCESSOR CONTROL (CPC)†

CPC provides displays of CPU P register(s), CPU breakpoint address, channel status, CPU and PPU program names, and exchange package and central memory displays. CPC controls starting and stopping of CPU(s) and provides test mode for troubleshooting.

CPC calls one overlay to CM address 61000 absolute and upon going into auto down-loads it into part of PP10 memory. This gives CPC the following modes of operation.

MODES

NOT AUTO	The mode that CPC originally comes up in with the PPUs waiting with their channels active and empty.
AUTO	The mode that CPC goes into after a CR. All PPUs are idled and the G and J displays are brought up.

MESSAGES

WRONG	Illegal entry.
NO OVL	Notifies user that the CPC overlay 1CP was not loaded from CM when going to auto. Program loading and execution will continue normally, but any command that is contained within the overlayed area will not execute.
LOC 0 NOT 0	Notifies user that absolute location zero (0) of CM is nonzero. The notation DS stands for deadstart because the condition is irrevocable from CPC.
ERROR CEJ XY	CPMTR has been entered with an exchange with CEJ/MEJ enabled. XY will be 0 if the exchanged-out program was from CPU 0 and 1 if the exchanged-out program was from CPU 1.
ERROR EXIT	An error exit occurred in not-auto mode with CEJ/MEJ disabled. Relative address 0 contains the error mode and address where the error mode occurred.

† Refer to auto.

CPU X STOPPED ERROR EXIT BIT YY SET	An error exit has occurred in auto mode with CEJ/MEJ disabled. X is the number of the stopped CPU, and YY is the error exit mode bit position.

KEYBOARD ENTRIES

1. Setting Optional Displays

   Enter: XY. (cr)

   (CPC) sets X display on left screen
   Y display on right screen

   Choices for X, Y = A, B, C, D, E, F, G, H, I, J, K, L

2. Setting Memory Display Areas

   Enter: XN, A. (cr)

   CPC sets field n of display X to display 10 words of memory from address A.

   X may be C, D, or E (refer to section 2)
   n may be 0, 1, 2, 3, 4
   n = four sets all fields

3. Enter Memory

   Enter: A, V. (cr)

   CPC stores value V in address A.

   Enter: LA, V. (cr) to left-justify entry

   Enter: A+V. for sequential storing of data

   NOTE

   The relative address RA is first added to A.

4. Enter CPU Register

   Enter: Rn, V. (cr)

   CPC stops CPU if running and enters value V into register Rn. (sets exchange package). R may be A, B, X, RA, FL, RE, FE, or MA, and n may be 0 through 7 for A, B, or X, while others do not require n. When RA is used, the FL value is automatically updated.

5. Enter Breakpoint Address

   Enter: BK , V. (cr)

   CPC sets breakpoint address to value V. That is, instructions at address V are saved and replaced with program stop.

6. Set CPU Control Mode

   Enter: Test. (cr)

   CPC sets up test mode where the P register is continually monitored for breakpoint address. When breakpoint address is reached, the CPU is exchanged out and exchanged back in with the following.

   a. If A display is selected, exchange-in is done with input package.

   b. If B display is selected, exchange-in is done with last output package.

   Enter: RUN. (cr)

   CPC sets up RUN mode where the CPU runs until breakpoint is reached. If breakpoint is reached, the CPU is exchanged out and breakpoint address is restored.

7. Set New Exchange Address

   Enter: EX, V. (cr)

   CPC sets exchange address to value V. RA and FL control in CPC are read from the new area.

   NOTE

   The relative address RA is not added to V.

8. Start Central Processor (Refer to CPMTR)

   Enter: Spacebar

   CPC exchanges central processor with the following.

   a. If B display is not selected, exchange is done with input package.

   b. If B display is selected, exchange-in is done with last output package.

9. Stop Central Processor (Refer to CPMTR)

   Enter: Backspace key

   CPC exchanges central processor with the following.

   a. If B display is not selected, exchange is done with input package with P and RA cleared.

   b. If B display is selected, exchange is done with last output package with P and RA cleared.

10. Clear Pause Bit and Start all PPUs Running

    Enter: Go. (cr)

    CPC clears the lower byte in CM address 100 and sets all PPUs running (under auto).

11. Change CPU Control (Dual CPUs only)

    Enter: Equal Key

    CPC sets displays and keyboard controls (RCP, DCP, TEST, RUN) for CPU-n.

    Enter: Equal key (=) to toggle back and forth between CPU-0 and CPU-1 control.

12. Load Program

    Enter: X.MNE. (cr) or X.MNE,CCUE. Enter channel and equipment to loaded PP or X.MNE,Z, X=PP to load under auto.

    CPC issues functions 0001 to LDR to load program MNE. Also, pause bit is cleared.

13. Transfer Central Memory to PPU

    Enter: MTP,X. (cr)

    CPC issues function 0002 to (LDR) to transfer program at CM address (RA+X+1) to the next available PPU. Address X upper byte must be nonzero.

14. Drop All PPUs under auto.

    Enter: DROP. (cr) (All PPUs that are running will be idled.)

15. Drop PPU under auto.

    Enter: X.DROP. (cr) Idles PPU X.

16. Memory Byte Entry (Dependent upon which memory display is selected)

    Example: E display up.

    CM. 100 = 7777 6666 5555 4444 3333

    Entry: 100,5,1234. will change the last byte (3333) to 1234.

    Example: C or D display up.

    CM 100 = 77777 66666 55555 44444

    Entry: 100,4,12345. will change the last byte (44444) to 12345.

17. X Register Byte Entry

    Example: X1 = 7777 6666 5555 4444 3333

    Entry: X1,5,1234. will change the last byte (3333) to 1234.

18. Set Memory

    Entry: SET,100,200,XXXX. will set all bytes to XXXX from location 100 up to and including location 200. If X is five characters long, four bytes will be set instead of five.

19. Cm. Cr clears central memory from 400 - protecting ra, fl, and ma for CPU 0 (in nonauto mode only).

20. Scan Memory

    Example: + entry moves all display 40 locations forward and - entry moves all displays 40 locations backwards.

21. (cr) - initial (cr) will bring in auto multiprogramming.

22. • Key as the first entry will abort the loading of a program from tape.

23. X.* will assign display to PPU X. Any later * command in auto mode will perform DIS function to assigned PPU.

24. (/) Slash entry will cause dayfile program (DMP) if running to dump accumulated buffer to the printer.

25. Right blank key will do a repeat entry.

26. CBPX (cr) - clears the CPMTR capability to loop on error CEJ conditions, X = CPU number. †

27. SBPX (cr) enables CPMTR to loop on an error CEJ condition, X = CPU number. A use program, monitor flag clear, exiting with any MODE error will be restarted using its INPUT exchange package. †

28. IR,xx (cr) enters the interlock register maintenance bits on CYBER 70. †

    Bit 0 = phase 1, bit 1 = phase 2, bit 2 = phase 3, bit 3 = phase 4
    To advance a phase, delay all others.

    EX. IR,15 (cr) advances phase 2
    EX. IR,4 (cr) delays phase 3

† These commands are valid only in stand-alone mode; they are not available in auto mode.

NOTE

This command is valid in stand-alone mode only. Use DLY in auto mode.

29. Right parenthesis key ()) enables and disables.

    a. A two-octal byte interlock register maintenance bit display to the right of the channel display (on CYBER 70 only).

    b. The CPMTR idle instruction at central memory location 3.

NOTE

The maintenance bit display must be off when running the test IRT in auto mode.

30. A series of commands to CYBER 170 interface MTR can be found in the CYBER 170 Supplement, publication number 60409500.

31. X.YYY,ZZZZ - CR enters PP memory address YYYY with data ZZZZ. The comma can be replaced with a plus for sequence storing. This is used mainly to change parameters in a super P interface program.

NOTE

This can be used for normal PS-interfaced SMM programs as long as ZZZZ ≠ to 0.

32. X.RUYYY - CR is used to start a super P - interfaced program (which can be identified by a / following the program name after loading) at PPU location YYY.

33. M,ZZZZ CR or X.M.ZZZZ CR will send the CPC keyboard buffer to DMP which will enter it in the I display and its central buffer to be printed with any test message.

NOTE

This is an excellant way to head error messages with date/time, special conditions, margins or delay probes, or parameter settings.

34. J=X, ZZZZ CR assigns the J display to PPU X. If the PPU responds, a PPU memory display will appear (if the J display is displayed upon either screen). ZZZZ is the memory address to be displayed (ZZZZ optional).

NOTE

At this time, only D44 is available to the J display.

35. JY, ZZ00 CR sets the areas of PPU memory to be displayed for the I display:

Y=0	Upper memory block
Y=1	Middle memory block
Y=2	Lower memory block
Y=3	Or
Y=4	All memory blocks with a 100B increment
ZZ	PP memory address to be displayed

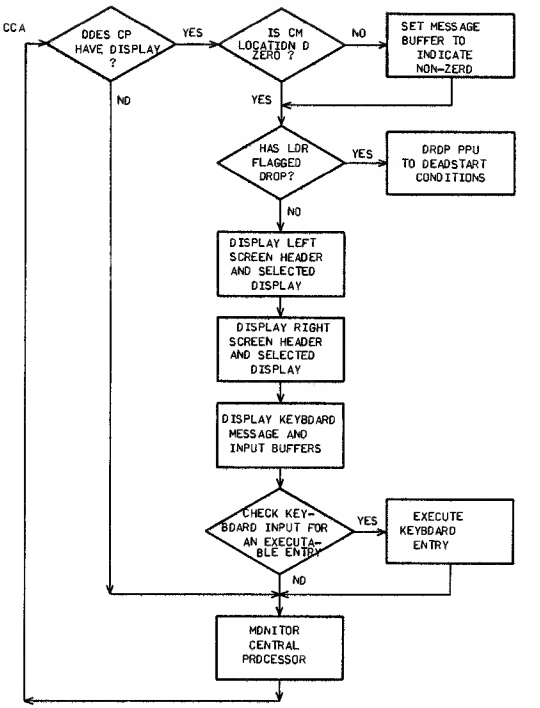
DISPLAYS

NORMAL DISPLAYS

CPC displays title line, LDR message line, status of I/O channels, and keyboard buffer on left screen at all times. On the right screen, CPU P register and mode and breakpoint address of selected CPU are displayed at all times. Also, on each screen is one of the following optional displays.

A Display	Both input and output exchange packages are displayed when CPU is stopped. Only input package is displayed when CPU is running.
B Display	Input exchange package.
E Display	Four fields of 10 CM words each are displayed. Words are displayed in five groups of 12-bit bytes. Displayed code conversions appear opposite octals.
D Display	Same format as C display, except locations displayed are incremented by 40_8.

C Display	Four fields of 10 CM words each are displayed. Words are arranged in four groups of 15-bit bytes.
F Display	Fake display, only lines described under normal displays appear on screen selected to display F.
G Display	Auto system display for multiprogramming.
H Display	Test list display. H display selected will display TL1-TL100
I Display	CPU message display. CPU REQUESTS I DISPLAY will be displayed.
J Display	J=0 displays CPC commands. J=X allows a PPU memory display for D44-type programs or a PPU driven CPC display such as the command display provided with J=0.
K Display	The K display is used on CYBER 170 in conjunction with MTR to display PPU memory, channel parity, transmission parity, and CSU SECDED errors.
L Display	The L display is used on CYBER 170 in conjunction with MTR to display CPU status, status control register, and SECDED error history.


CCA
DOES CP HAVE DISPLAY ?
YES
NO
IS CM LOCATION D ZERO ?
NO
SET MESSAGE BUFFER TO INDICATE NON-ZERO
YES
HAS LDR FLAGGED DROP?
YES
DROP PPU TO DEADSTART CONDITIONS
NO
DISPLAY LEFT SCREEN HEADER AND SELECTED DISPLAY
DISPLAY RIGHT SCREEN HEADER AND SELECTED DISPLAY
DISPLAY KEYBOARD MESSAGE AND INPUT BUFFERS
CHECK KEY-BOARD INPUT FOR AN EXECUTA-BLE ENTRY
YES
EXECUTE KEYBOARD ENTRY
NO
MONITOR CENTRAL PROCESSOR

CENTRAL PROCESSOR MONITOR (CPMTR)

PURPOSE

Provides a program to do the following.

1. Get the CPU out of monitor mode after execution of CPU -XJ instruction or PP MXN or MAN (if P is not 0 or 1 on entry to CPMTR).
2. Handle error CEJ:
   a. Move exchanged-out program to output exchange package area.
   b. Set up either an idle exchange package or A.
   c. Means of reinitiating a program that error CEJ exists (that is, exchange to rerun the program setting up a loop on error CEJ condition).
   d. Clear the monitor flag by an XJ to BJ.
   e. Signal CPC that an error CEJ has occurred.

In addition, provides a means of starting and stopping a CPU, using an MXN/MAN exchange as an installation parameter as opposed to EXN exchange control from CPC. This simulates operating system operation more easily as all CYBER systems and many 6000 systems use MNX/MAN operating systems. The 742X CYBER systems have a defined hardware problem where an EXN to one CPU, interrupting the other CPU executing a CEJ or ECS instruction, will hang chassis 5/9 requiring a deadstart to clear.

NOTE

CPMTR will remain the same for all three options; only the code in CPC will change.

Also, provides CPC with an ECS display capability.

ENTRY

CPMTR can be entered by an MXN, MAN, XJ, or error CEJ CPU MA=340, CPU1 MA=360.

A CPU program may change MA by setting up a call to CPMTR in its RA+1, and exchanging into monitor state with B1 = its RA. The following format for RA+1 is used.

Upper 24 bits = new MA
Lower 18 bits = CMA

Upon reentry to program, A6, B6 will be destroyed.

COMMUNICATION

SIGNAL	Signals error CEJ to CPC.
COUNTER	Counter that tells how many times CPMTR has been entered.
BKP	Should be set to nonzero to cause a program that exited CPU0 with an error CEJ to be reinitiated.
EXCHADRA	CPU0 input exchange package address.
EXCHADRB	CPU1 input exchange package address.

USAGE

HANDLE ERROR CEJ

If a program should encounter any of a number of error conditions on a CYBER 70 mainframe with the CEJ switch enabled (and no disabling ground caps or wires), an error sequence is started. First, the error mode and address at which it occurred are stored in RA, then a CEJ is performed. This CEJ, which is a result of any error exit condition, will be designed as an error CEJ. This error CEJ uses MA for the exchange address and will set the monitor flag. The monitor exchange package resides at the address specified by MA when the monitor flag is clear. In CPMTR, the P register from the exiting user program is tested for 0 or 1 (0 = 74XX exit, 1 = 73XX). If either of these conditions is true, CPMTR will move the user program output exchange package (which replaced the monitor package in memory at MA when we exchanged) to the user output exchange package area, (exchange address + 20, normally 420 for CPU0). CPMTR then creates an

idle exchange package in the monitor exchange area and CEJs (BJ+K) to it. This puts the CPU into user mode (monitor flag clear) and executes an idle program. Coincidently, the monitor package is moved from the CPU back to its monitor exchange package area in central memory. At this point, CPMTR signals CPC of the error CEJ that it has processed. CPC then clears the CPU running flag in the PP and issues the message ERR CEJ XY, where x = 0 indicates CPU0 and Y=1 indicates CPU1 (both could possibly be up concurrently).

NOTE

MA is preset to 340 for CPU0 and 360 for CPU1.

HANDLE CONFLICT CEJ, MXN, AND MAN

If a CE wishes to add conflicts to an executing CPU program in the form of a CEJ, simply insert the CEJ anywhere in the main line of the program. The CE or user program on encountering the CEJ will exchange to MA and follow much the same path as stated in error CEJ, except the user P register will not be equal to 0 or 1. To clear the monitor flag and restart the user program, CPMTR executes a CEJ to BJ+K. This initiates the user program at the execution address + 1 of the conflict CEJ.

MAINTENANCE BITS CONTROL ROUTINE (DLY)

INTRODUCTION

This routine controls the maintenance bits of the interlock register. It is a maintenance aid which allows control of the various clock phases. It runs under SMM 6000/CYBER.

OPERATIONAL PROCEDURE

RESTRICTIONS

1. Runs under auto only.
2. Runs only on CYBER machines (72, 73, 74) and 6000 types with QSE for the interlock register. Routine will exit if channel 15 is nonexistent.

PARAMETERS AND/OR ENTRIES

1. All entries are displayed on the left screen after DLY has been loaded.
2. Location 70 = delay time (that is, the time before a clock phase change is made). This time is in milliseconds per count.

   Entries

   P1 = Phase 1 test point 6 delayed
   P2 = Phase II test point 1 delayed
   P3 = Phase III test point 2 delayed
   P4 = Phase IV test point 4 delayed
   A1 = Phase 1 test point 6 advanced
   A2 = Phase II test point 1 advanced
   A3 = Phase III test point 2 advanced
   A4 = Phase IV test point 4 advanced
   ON = Display PPU memory on both screens
   OF = Do not display PPU memory
   RR = Change clock phases randomly at a rate determined by (70)
   TM = Toggle mode, toggle between phase selected and no advanced or delayed phase
   AC = Clear all bits of the interlock register
   AA = Set all maintenance bits

MESSAGES

The messages displayed coincide with the following typeins.

Typein	Message
P1	PH 1 DELAYED
P2	PH 2 DELAYED
P3	PH 3 DELAYED
P4	PH 4 DELAYED
A1	PH 1 ADVANCED
A2	PH 2 ADVANCED
A3	PH 3 ADVANCED
A4	PH 4 ADVANCED
AC	ALL MAINT BITS CLEAR
AA	ALL MAINT BITS SET

DAYFILE AND MEMORY DUMP (DMP)

INTRODUCTION

This is a line printer dump routine used to dump PPs and central memory without the need to deadstart DDD. Also, dumps the SMM (auto) dayfile.

Runs under SMM (auto) mode.

OPERATIONAL PROCEDURE

RESTRICTIONS

1. Runs under SMM (auto) mode only.
2. The PPU that is to be dumped must not be in a hung state; may be idle.
3. PP0 and PP8 cannot be dumped.
4. Cannot dump PP if printer channel = communication channel.
5. Illegal to run two copies of DUMP. Dropping one copy will clear interface flag with PS package which disables remaining copy.

LOADING PROCEDURE

Called into a PP by X. DMP. Must be called into a PP number less than EXCs PP number.

PARAMETERS

All parameters are displayed on the console. Type X. DIS. to look at parameters.

MESSAGES

DUMPING CENTRAL MEMORY	While dumping CM
DUMPING PPX	While dumping PPX
PPX CANNOT BE DUMPED	The PP is not communicating with the SMM system. Restart DMP. Type R or try and free the PPU through channel entries from CPC.

LP NOT READY	The line printer is not ready. Check paper-out condition.
SET LOC 1502 = LP(CCEE)	Displayed at beginning of dump routine. Parameters may be changed at completion of any dump.
DUMPING DAYFILE TO CM	Displayed during monitor of the dayfile.
TYPE CF--F, L--L, R--R. TO DMP F TO L RELATIVE TO R	Dump CM from address (F--F) to address (L--L) relative to address (R--R).
SET LOC 1500 = 2000 - DO NOT DUMP DAYFILE TO I DISP.	
SET LOC 1500 = 4000 - DO NOT DUMP DAYFILE TO CM	
DAYFILE RQ I DISPLAY	

NOTE

Type GO- if any hangups occur because of paper out, not ready, etc.

I DISPLAY RESTRICTIONS

The I display, under auto (generated by DMP) can be destroyed by any test call which loads to central memory locations 20000_8 through 20777_8.

Examples:

```
PP1   DMP    (W/I display)
PP2   EXC
```

or

```
PP1   DMP    (W/I display)
PP2   MM4
```

or

Loading a CPU test (CU3, CM6, etc.) with an RA < 21000_8

6000/CYBER 70/CYBER 170 MULTIPROCESSING ROUTINE (EXC)

OPERATIONAL PROCEDURE

LOADING

This routine loads under the multiprogramming mode (auto) of the 6000/CYBER 70/170 SMM using the mnemonic EXC or EXC,XXYY, where XX is unused and YY is the starting RA under EXC in units of $10,000_8$ words.

PARAMETERS

Entry	Description
EX,WWWW.	Change exchange rate to WWWW. Defaulted to 20 which is 58 microseconds.
CFL,X,YYY.	Change field length of program X (X=A through T on the left display) to $YYY/100_8$.
TL,T1,T2, T3,T4.	Load tests T1, T2, T3, and T4 (must be at least two tests). Some tests may be selected more than once.

Single-Character Entries

The following entries may be entered anytime.

Entry	Description	Default
+	Add ECM to random test	Off
-	Delete CT3 from random test list	Off
*	Toggle stop on error	On
(	Toggle automatic rate change	On
)	Toggle DDP with ECM	Off
=	Toggle random select	Off
†7	Select EM=7000	On
†0 (zero)	Select EM=0000	Off
D	Return display to CPC	
S	Stop	
Space	Start	
F	Toggles display on and off	

† CYBER 17X only.

MESSAGES

CPU X RA XXXXXX, FL= YYYYYY

This initial messages gives the central memory relative address (RA) and field length (FL) available for programs that will run in CPU X. Under CPC, an N.GO (N=PPU number) may be entered, and the default parameters given previously will be used. The parameters may be changed before or during execution by assigning the display to EXC (N.*).

MNE=WWWWWW MNE=XXXXXX MNE=YYYYYY
MNE=WWWWWW

This message displays the current P addresses of the running programs.

PROG x MSG YYYY

An error message, YYYY, is being reported by program number X if stop error is selected.

PROG x MSG MODE 0 AT ZZZZZZ

Program X has taken an error exit at address ZZZZZZ. This error message usually indicates that on a CYBER mainframe the program halted by executing a program stop (PS) instruction and has executed a central exchange jump (CEJ) to the monitor address (MA).

LOADER/MONITOR (LDR)

LDR monitors PPU output registers for call codes for LDR action. LDR performs the following operations in response to the call codes.

Call Code	LDR Action
0001	Load program.
0002	Transfer central memory to PPU.
0003	Not used
0004	Load overlay to CM library.
0005	Deadstart LDR and CPC PPUs.
0006 through 0011	Refer to auto.

1. Load Program - Code 0001

   This call causes a program to be loaded from tape. Tape will be searched, if necessary.

   a. Keyboard Entry

      X. MNE. (cr)

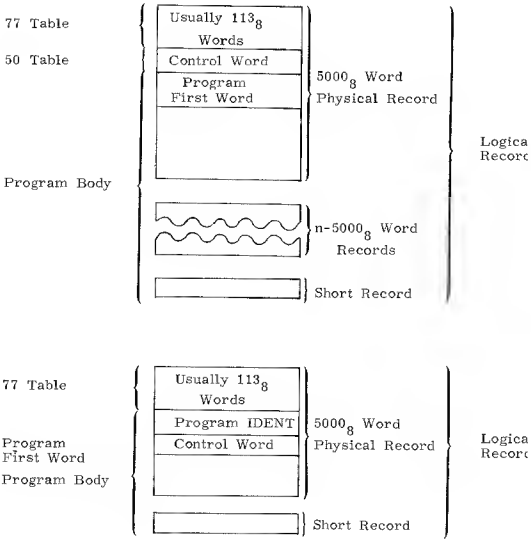
   b. Call Format

      CM Address 101 = 0001 0000 0000 0000
      0000 (Output register)
      102 = MMNN EE00 0000 0000
      0000 (Message buffer)

   c. LDR Action

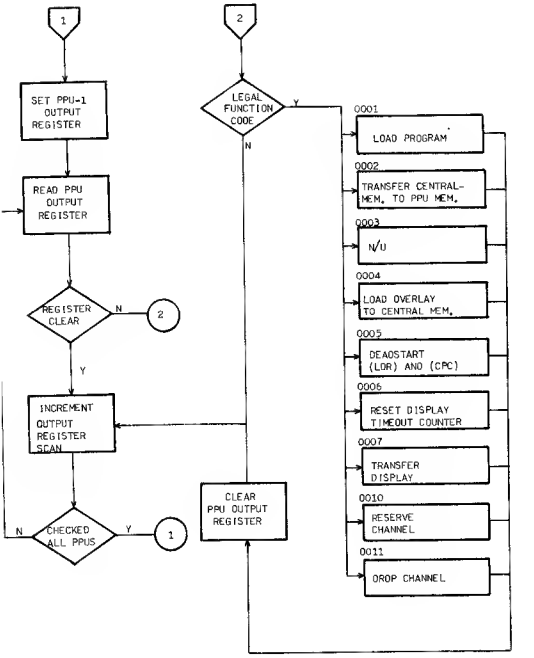
      LDR rewinds and searches the SMM tape for the program whose mnemonic is left-justified in the calling PPUs message buffer, CM address 102 for PPU8. If the end of file is reached, the message NOT IN DIRECTORY is written into CM address 103 to be picked up by CPC. If the program is found, its 77 table is stripped (usually 113 PPU words) and control word determines disposition of the record. CPU programs are identified by a five-word 50 table (refer to SCOPE Reference Manual, loader operation) which follows the 77 table. PPU program disposition is determined by the value of the programs first-word address which immediately follows the 77 table.

CPU PROGRAM LOGICAL RECORD



NOTE

A logical record does not necessarily contain one 5000_8 word record. The idea is that it ends on a record length less than 5000_8 words.


1
SET PPU-1 OUTPUT REGISTER
READ PPU OUTPUT REGISTER
REGISTER CLEAR
N
2
Y
INCREMENT OUTPUT REGISTER SCAN
CHECKED ALL PPUS
N
Y
1
2
LEGAL FUNCTION CODE
Y
N
CLEAR PPU OUTPUT REGISTER
0001
LOAD PROGRAM
0002
TRANSFER CENTRAL-MEM. TO PPU MEM.
0003
N/U
0004
LOAD OVERLAY TO CENTRAL MEM.
0005
DEADSTART (LOR) AND (CPC)
0006
RESET DISPLAY TIMEOUT COUNTER
0007
TRANSFER DISPLAY
0010
RESERVE CHANNEL
0011
DROP CHANNEL

Control Word	Program Type	(LDR) Action
0001	PPU-1	The program is shipped to the next available PPU, initially PPU-1. The program executes at address 2.
5000	CPU	Program is loaded into central memory at a relative address specified by CPC, initially 10000_8.
0000	PPU-0	CPC is requested to drop and to deadstart PPU-8. The program overlays LDR in PPU-0 and starts execution at address 1.
0001	PPU-1-7, 9-19	Refer to auto.

2. Transfer Central Memory to PPU - Code 0002

   This call provides a method to enter an octal PPU program in central and then transfer it to a PPU.

   a. Keyboard Entry

      MTP, XX, (CR) XX is CM address.

   b. Call Format

      CM Address 101 = 0002 0000 0000 0000 0000

      CM Address XX = MMNN EE00 0000 0000 0000

      MMNNEE is the program mnemonic; must be nonzero.

   c. LDR Action

      LDR transfers 1462_8 CM words from CM address XX+1 biased by RA as set by CPC to the next available PPU-1. The program starts at the value +1 of the upper byte of CM address XX+1.

3. Unused Function

4. Load Overlay to CM Library - Code 0004

   This call facilitates loading of overlay segments into a central memory library when a PPU overlay program is loaded. The call is normally used by the PS interface.

   a. Keyboard Entry

      None

b. Call Format

CM Address 101 = 0004 0000 0000 0000 0000
102 = MMNN EE00 0000 0000 0000

MNE is overlay segment mnemonic.

c. LDR Action

NOTE

If the calling PP is greater than the PP in which EXC resides, then the call is replaced by a drop function.

LDR searches the SMM tape for segment MNE and loads it into the overlay library which starts at CM address 1000_8. Each segment loaded is prefaced with an entry control word. The following format is used.

Entry	Word	MMNN EE00 FFFF EEEE LLLL
Where	MNE	Segment mnemonic
	F	Entry first-word address in library
	E	Ending address in library
	L	Length of segment in CM words

5. Drop LDR and CPC - Code 0005

This call gives PPU programs the ability to drop SMM control.

a. Keyboard Entry

None.

b. Call Format

CM Address 101 = 0005 0000 0000 0000 0000

c. LDR Action

LDR requests CPC to drop; PPU-8 will go to deadstart conditions. LDR sets PPU-0 to deadstart conditions. This operation is completed when the call register is cleared by LDR.

ADDITIONAL FEATURES

1. SMM can be initialized by loading LDR from the card reader when SMM is on a disk or drum. The disk/drum parameters are in words 13 and 14 of the deadstart panel. Requires PCL loader card to load LDR. (Refer to writeup.)

2. Deadstart exchange in CPU.

   In the case of CPU hangups, do a deadstart exchange of CPU0, CPU1, or both.

   a. Do a normal deadstart to get CPC display.

   b. Set up the CPU program you want to execute under the CPC A display.

   c. Change the deadstart panel to the following.

      1 - 0100
      2 - 0100 LJM 100 D.S. EXCH CPU0
      3 - 0300 HANG PP0 (LDR)

      To deadstart exchange CPU1, change location 2 to 0120.

   d. Put the deadstart switch in the D.S. position (ON); every deadstart will exchange the CPU.

   e. To start both CPUs, use the following deadstart settings.

      1 - 0100
      2 - 0100 GO EXCH CPU 0
      3 - 0100
      4 - 0120 GO EXCH CPU 1
      5 - 0300 4awg PPU 0

   NOTE

   LDR transfers the input PKG to the output EXCH PKG area (400 to 420 for CPU0, 600 to 620 for CPU1), then exchanges the CPU with the output EXCH PKG. A normal exchange jump (2600/2601) instruction is used for the exchange. LDR exits to location 3 of the deadstart panel.

3. Before calling CPC to PP10, LDR loads CPMTR to CM addresses 247-377.

4. LDR now loads the exchange package associated with a CP test being loaded to the exchange address set for the appropriate CPU.

   Example: EX,200000

   or

   FST

   or

   SPACEBAR Allows a CPU program to be started by an exchange to the upper banks on a CYBER mainframe.

5. MA is preset in the input exchange package to 340 for CPU0 and 360 for CPU1.

6. FE is preset to run ECM.

7. PSM can now be loaded to PP12-23 while in NOT AUTO.

8. SMM can now reside on one 844 pack for several mainframes to access concurrently (DUAL ACCESS).

FULL ADDRESSING FOR CENTRAL MEMORY UTILITY PROGRAM (FAD)

DESCRIPTION

FAD is an auto mode multiprocessing utility program. When FAD is called, it enters a PPU and writes all of central memory with an address pattern (that is, each location contains its address as data) in one of three modes. Central memory is written from a low address to the last address in memory. The last address is obtained by FAD from word 1 of central memory which can be altered under CEL/ENS using an SYxx,yyyy command. Once it has completed addressing memory, it releases the PPU back to SMM in the idle state.

USAGE

The various modes of FAD are called by typing one of the following under the auto mode display.

FAD·cr or FAD,0·cr — This command causes FAD to load and write addresses in central memory from absolute address 360B to the end of central memory.

Example: location 1001=0000 0000 0000 0000 1001

FAD,1·cr — This command causes FAD to load and write addresses in central memory from the RA given in the exchange package at location 400B to the end of central memory. Do not use if RA .LT. 1000B.

Example: location RA+74576 = 0000 0000 0000 0007 4576

FAD,2·cr — This command causes FAD to load and write jump instructions to the current address in central memory from the RA given in the exchange package at location 400B to the end of memory. Do not use if RA .LT. 1000B.

Example: location RA+36574 = 0200 0365 7400 0000 0000

FAD, 3•cr	This command causes FAD to load and halt at the parameter stop message. Unless the parameter at location 1502 remains unchanged, the go command causes FAD to do nothing but loop back to the parameter stop message.
FAD, 4•cr through FAD, 7•cr	These commands cause FAD to load and execute in the same manner as FAD, 0 through FAD, 3 respectively, except that a parameter stop occurs first.

MESSAGES

SET PARAMS - mm/dd/yy	This message is displayed at parameter stop only. This message must be displayed if the user desires to use an n• DIS command. The mm/dd/yy represents the month, day, and year of the latest assembly of FAD.
SETTING FULL ADDRESS	This message is displayed to indicate that FAD is currently running (that is, executing) commands FAD, 0 through FAD, 2.

PERIPHERIAL SERVICE MULTIPROGRAMMING ROUTINE (PSM)

SMM CALL

PSM,ABCD. CR where 1502=ABCD after loading.

NOTE

Location 0045=3000 after loading.

PURPOSE

PSMS creation was influenced by the following items.

1. Encourage CEs in the field to write peripheral programs, since this leads to a more thorough understanding of the equipment and gives the CE a better feel for operating system problems.
2. Retain as many PS interface package features as possible; the CE should already be familiar with its operation and use.
3. Incorporate as many service routines as possible from PSP for use under auto, because they have already proven their usefulness in the field.
4. Enable a peripheral program to run simultaneously with a central program under SMM control.

OPERATIONAL PROCEDURE

DISPLAY

1. The PPU memory display can be changed the same as the PS interface (that is, 0200W20AA, 0204W20AA, 0210W20AA, 0214W20AA, where AA X 100 is the location to be displayed).
2. A programmer can create his own messages on the left screen by calling one of the three standard PS message displaying routines. (Refer to use of message options.)
3. Selectable CPC G display for monitoring other PPs while programming a PPU.

KEYBOARD ENTRIES

The following entries do not require carriage return.

F	Clears and returns the PP memory display from the right screen (used to speed up program execution).
G	Starts program execution at the address specified by the contents of location 0045 (same as PSP).
S	Stops program execution by returning the program to the display loop.

NOTE

If a programmer has been displaying a message, this message is cleared from the screen and a normal PSM display will replace it. Therefore, if a programmer is displaying his own messages, an RJM-PS. MSGS should be used to stop program execution. If this is done, a SPACE or GO from SMM will continue the program following the PS. MSGS call.

)	Ends PSM and idles the PPU.
=	Enables sequence storing when used anytime after a valid octal input (need not be the fifth entry). Example: 20=XX CR or 3000=XXX CR
+	Increments by 100 the locations displayed by the first three PP memory displays (anytime).
-	Decrements by 100 the locations displayed by the first three PP memory displays (anytime).
D	Drop; returns the display to CPC (anytime).
/	Allows the programmer to insert data or code at any address while shifting all codes above that location up one location.

NOTE

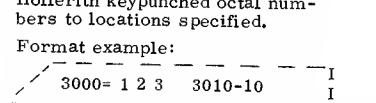
No attempt is made to correct any code that references an address within the shifted area.

RIGHT BLANK KEY	Toggles the left display between the instruction and CPC G displays (use to monitor how other peripheral tests are progressing while writing a program).
BACK-SPACE	Clears the last keyboard entry.
SPACE-BAR	If it is the first entry: 1. And no message call to PS. MSGS has been made by the programmer, then 3000B is stored in location 0045 and program execution is started at location 3000. 2. If a message call to PS. MSGS has been made, then program execution continues at the next instruction after the RJM-PS. MSGS. If other than the first entry, it is a delimiter.
LEFT BLANK KEY	Clears keyboard entry pointer, clears sequence storing flag, and clears keyboard message flag.
CR	As the first entry, sets repeat entry flag. Otherwise, executes the command entered.

SERVICE ROUTINES

RBCCXE, YYYY, ZZZZ CR	Reads absolute binary cards from channel CC, equipment E to PPU location YYYY, where ZZZZ is the number of cards (octal count).
LOCCXE CR	Loads octal cards routine. Loads Hollerith keypunched octal numbers to locations specified.

Format example:



Results:

```
3000=0001
3001=0002
3002=0003
3010=0010
```

=	Immediately following an octal number, reset the address to wbich the numbers following the = sign are sequence-stored.
SPACES	Acceptable delimiters. Any number can be used between entries.
"."	Signifies end of information and routine will continue reading until one is encountered.

NOTE

Data is sequenced-stored if a new address is not specified each time. There is no limit on the number of cards that can be input.

PBCCXE, YYYY, ZZZZ CR	Punches absolute binary cards. (Refer to RB ROUT.)

NOTE

A MAC will be assumed by the previous three routines on the channel specified by CC if DF.1015 (MAC code) has been enabled in PSM and then X is defined as the MAC number.

CM CR	Clears PP memory from 20 through 67, 3000 through 7777, and resets location 0045=3000.
RCAAAA, BBBBB, CCCC or RCAAAA, BBBBB, CCC or RCAAAA, BBBBBBCCC	Reads central memory to PPU address AAAA from central address BBBBBB, where CCCC is number of central words (octal count).

NOTE

Any central address can be referenced by this routine and delimiters are not needed. PP address is four numbers, central address is six numbers, and word count is one through four numbers.

WCAAAA,BBBB, CCCC or ETC.	Writes central memory. Refer to RC routine for format and use.
CHDDDD,EEEE, FF CR	Changes channel routine, which will change the channel number of any channel instruction from location DDDD for EEE number of locations, where FF = channel number.
WPGGGG, HHHH,IIII CR	Writes pattern in PPU memory from address GGGG for HHHH number of words, where IIII is the pattern.
RWJ.CCOE CR	Rewinds tape unit J on channel CC, equipment E.

NOTE

This routine can also be used as a connect routine.

ULK,CCOE CR	Unloads tape unit K on channel CC, equipment K.

NOTE

If code is not specified in the previous two routines, then the deadstart channel and equipment are substituted.

If DF.1015 (MAC code) is defined to PSM, then the previous two routines do not exist.

PROGRAMMING CONSIDERATIONS

(Use 20 through 67, 1500 through 1510, 3000 through 7777.)

PSM communication with CPC/LDR, ending a program with:

1. An LJM-232 executes the program once and then returns to the display loop.
2. An LJM-236 will loop through a program while retaining system communication.
3. An LJM-100 is illegal at anytime because system communication will be lost.

Once a program has been started, either by a SPACE, G, or X.Go., the point at which the program will be entered can be changed by storing the new starting address in location 0221.

The request and release channel routines should be incorporated in your program if there is any chance that another PPU may become active on a channel you are using. Previous to making use of these routines, store 1502-CCXX, where CC is channel number and XX can be anything. To request a channel, do an RJM-1141 and to release the channel, do an RJM-1161.

If a 6681 or 6684 is present on the channel you wish to drive equipment on, issue a (77CC-2000) connect before trying to connect the equipment. Although the 81 and 84 are connected on deadstart, SMM diagnostic program DF selects them after use.

If a programmer should wish to completely take over the display console and associated keyboard input, then a REQUEST DISPLAY (RJM-325) must be done before any instruction can be executed on the display channel.

Use of the message option. If a programmer wishes to replace the RUNNING message with an informative or error message both in the PPU and in the CPC G display, then use one of the following routines.

PS.MSG	Displays message on the left-hand screen and PPU memory on the right screen. RJM-1030.
PS.MSGS	Same operation as PS.MSG, except PSM will stay in the display loop until the SPACEBAR is hit or a GO is received for CPC. RJM-1061.
PS.CPMSG	Same as PS.MSG, except no PPU memory display. RJM-1046.

To make use of any of these routines, simply load A with the address of the first location of the message you wish to display (which must end with a word of zeros) and do a return jump to one of the message routines.

NOTE

Besides displaying a message, the message routines carry on normal communication with LDR/CPC. Also, if 10000 is added to the message address, then DMP will pick up message.

Example 1:

```
3000-2000
3001-3100
3002-0200
3003-XXXX
3004-0100
3005-3000
```

Load A register with address of the information to be displayed, and then do a return jump to one of the display routines. Either loop on your program or jump to 232 or 236.

Example 2:

```
3000-2001
3001-3100
3002-0200
3003-XXXX
```

Adding 10000 to message FWA enables DMP to pick up the message; jump to message routine.

If the RB, LO, PB routine halts without clearing the keyboard display buffer and returning the PPU display to the right screen, one of the following conditions may exist.

1. LO routine has not found a period on a card read, and card reader is not ready.
2. RB routine has not yet read the number of cards specified, and the reader is not ready.
3. PB routine has not yet punched the number of cards specified, and the punch is not ready.
4. Any of the three routines have found the channel active after a function 2000, peripheral equipment rejected the connect attempt, 6681 rejected or had transmission parity set during transfer.

To correct any of the above conditions, type S to stop the program, F to return the PP memory display, and then drop back to CPC. If PSM still has the channel reserved and the channel is full, then condition 4A. If the channel is reserved and appears to be running, then conditions 1, 2, or 3. If the channel has been released, then conditions 4B or 4C.

KEY LOCATION CALLS

PS. PAUSE Checks for system abort, stop, go, and parameter entry flags. Does not call RCH or DCH.

Example:
```
RJM     PS. PAUSE+1
RJM-1262
```

PS. RCH Requests the channel number contained in MCP+2 (1502) from the SMM system. If the program has not separated a call to RCH by a call to DCH, no operation will be done.

RJM-1141

PS. DCH Operates the same as a call to PS. RCH, except it releases the channel to the SMM system.

RJM-1161

PS. CPMSG Displays a message on the left screen only. If DF. MLP has been defined, the message will be sent to PPS message buffer in central memory. Call PS. PAUSE and control is given back to the program. The message to be displayed may be any length, as long as each new message contains its own coordinates. The entire message must terminate with a 12-bit word of zeros.

EX. 1
```
        LDC     DIS1
        RJM     PS. CPMSG+1
RJM-1046
```

NOTE

If you wish the initial message to be sent to the SMM dayfile, add 10000B to the display FWA.

Example:

```
LDC  DIS1+10000B
     DIS1   DATA  H*RUNNING SEC1*
            DATA  6000B,7200B
            DATA  H*STATUS=XXXX*
            DATA  6000B,7300B
            DATA  H*TEST ALL UNITS*
            DATA  0
```

EX. 2
```
        LDC   DIS2
        RJM   PS. CPMSG+1
DIS2    DIS   ,*RUNNING
               SEC2*
              60299500 F
```

PERIPHERAL SERVICE ROUTINE (PSP/PSQ)†

DISPLAYS

RIGHT SCREEN

A, B, C, D, is displayed from top to bottom.

To change:

A display	Ayyyycr or Acr increments by 100 or 0200x20xxcr
B display	Byyyycr or Bcr increments by 100 or 0204x20xxcr
C display	Cyyyycr or Ccr increments by 100 or 0210x20xxcr
D display	Dyyyycr or Dcr increments by 100 or 0214x20xxcr Eyyyycr or Ecr

Eyyyycr will set A to yyyy and B and C 100 greater, respectively.

Ecr will increment A300 and B and C 100 greater, respectively.

cr = carriage return, xx = address in 100ths, yyyy = address (lead zero may be omitted).

LEFT SCREEN

Top line	PPO* Channel status
Middle	Description
Bottom	Keyboard display

*PPO = PPU number PSP is running in.

INPUT

KEYBOARD

1. If first character is numeric, format is xxxxzyyyycr. xxxx = address to store at, yyyy = contents (yyyy leading zeros not needed), z = any character
2. If first character is alpha, format is shown for each routine.

† PSQ is PSP for 3245 controller.

Single Character

G Execute program stored at address contained in address 45. or 0221xyyyycr.

yyyy = address (leading zeros may be omitted)

F Remove displays from right and left screen, except for channel status and keyboard input.

F Restore displays.

S Stop running program if looping through PST. or 0221x0232

* Set sequence storing.

* Clear sequence storing.

Blank keys	Clear keyboard display.
Backspace	Clear last keyboard entry.
Carriage return	Terminate keyboard input.
Comma	Separator between numerics.

To loop on the program, jump back to address 0236 to retain display.

To execute the program once, jump back to address 0232 to retain display.

ROUTINES

Leading zeros may be omitted, four numbers maximum between commas.

CM

Clear PPU memory addresses 0 to 37 and 3000 to 7777.

Format: CMcr

PP

Transfer PSP to PPU requested and display PPU number top of left screen.

Format: PPxcr x = PPU number

PM

Read 200 words from PPU memory requested, starting at address specified and display right screen in A and B.

Format: PMx,yyyycr x = PPU number
yyyy = Starting address

RB

Read binary cards.

Format: RBcheq,yyyy,ccccr

cheq = Channel/equipment	Exam: 1204
yyyy = Starting address	Exam: 3000
cccc = Number of cards	Exam: 2

NOTE

Cheq may be substituted with a comma if card reader is 1204.

PB

Punch binary cards.

Format: PBcheq,yyyy,ccccr

Same as RB.

NOTE

Cheq may be substituted with a comma if punch is 1307.

CC

Copy card from reader to punch of two consecutive end-of-file cards (column 1, 6789 punch).

Format: CCcheq,cheqcr

cheq = channel/equipment

First cheq is card reader (comma if card reader is 1204). Second cheq is punch (comma if punch is 1307).

NOTE

After RB, PB, or CC is done once, do not type in cheq until PSP is reloaded.

WC

Write central memory.

Format: WCxxxx, yyyy, wwwwcr

xxxx = PPU starting address
yyyy = Central memory address
wwww = Number of central words

RC

Read central memory.

Format: RCxxxx, yyyy, wwwwcr

Same as WC.

WP

Write pattern in PPU memory.

Format: WPxxxx, nnnn, pppp

xxxx = PPU starting address
nnnn = Number of words
pppp = Pattern to store

Addresses 42, 43, and 44 are the translated values from keyboard input for the following routines.

PP, PM, RB, PB, CC, WC, RC, WP.

CH

Channel insertion option (PSP only).

Format: CHXXXX, YYYY, ZZ.cr.

zz = The channel number to be added to all I/O instructions from location XXXX, up to XXXX+ YYYY.

PERIPHERAL SERVICE ROUTINE (PST)

PURPOSE

Provides certain I/O service routines under SMM and enables a peripheral program to be run simultaneously with a central program under SMM control.

OPERATIONAL PROCEDURE

The program runs under SMM control or deadstart from a card deck. After program loads, type X.DIS, where X = PPU number.

PARAMETERS

Routines may be started and parameters entered as indicated on the display. All entries (except G and S) must be ended witb a carriage return.

SPECIAL OPTIONS

S	Stops execution of a routine.
G	Restarts execution of a routine.
ON	Forces a memory display during execution.
OFF	Restores normal off mode of memory display during execution.
DCnn	Disconnects channel nn.
MCnn	Executes a master clear function (1700B) on channel nn.
CC	Returns to central display.

Connect codes for 3000 type equipments may be set by entering the Chippewa mnemonic for the equipment followed by a one- or two-digit channel and a single-digit equipment code.

Example: CR125 sets card reader to channel 12B equipment 5.

Status displays are self-explanatory, except the abbreviation RD represents read equipment and WT represents write equipment.

Automatic incrementing and decrementing of peripheral store addresses may be obtained by using the + and - keys.

The 53B blank key clears the entry line.

Leading zeros may be deleted on all data entries, except the addresses.

EXECUTION

If a program is started by entering 0221, XXXX will remain running (provided it returns to 0236) when control is given to CC (central display).

PERIPHERAL SERVICES (PSX)

PSX is a 3000 peripheral service routine designed to allow the CE to make alpha keyboard entries to accomplish various I/O tasks. It runs under SMM, auto mode, or SCOPE.

KEYBOARD ENTRIES

Entry	Function
RQCXX.	Sets up PSX to use channel XX; this must be the first I/O entry word.
RLCXX.	Releases channel XX to SMM for use by another PPU.
FCHX.	Functions the channel/6681 with function X.
CONX.	Connects equipment on requested channel [X=connect code and (A) = 6681 status] .
FNCX.	Functions equipment with function X [(A) = 6681 status] .
OUTX.	Outputs X number of words from location 7000 [X may be 1 through 1000 and (A) = equipment status] .
INPX.	Inputs X number of words to location 6000. 1500 read mode is used [X may be 1 through 1000 and (A) = equipment status] .
EST.	Takes equipment status and displays on left screen C=XXXX [(A) = equipment status] .
CST.	Takes 6681 status and displays on left screen C=XXXX [(A) = 6681 status] .
B,XY	Transfers X buffer to Y buffer area (X=I, O, P) (Y=I, O, P).
PXXXX.	Sets P address of PPU to XXXX.
MFXX.	Sets right screen memory display field F to XX times 100. F may be A, B, C, or D.
ENT,F,L,X.	Sets X in PP memory from location F to location L.
XXXX.	Sets XXXX in PP memory at current P address.
D	Releases display to SMM (CPC).

Entry	Function
G	Starts program (which is in test mode) and makes one pass starting from location 5000.
SPACE	Starts program (which is in test mode) from location 5000 and runs until S key is depressed.
S	Stops program running in test mode.
T	Sets test mode.
(CR)	Sets repeat entry flag.
Blank (55)	Clears test mode flag and resets P address to 5000.

OPERATION

If test mode is not set, all I/O entries are executed as they are entered.

6681 status (C), (E) equipment status, and the current (P) address are displayed at all times.

If test mode is set, all I/O entries are stored in the current P address area (5000 through 5777) and not executed until a G or a space is entered. P is automatically updated for each entry made. Octal entries (XXXX.) may be mixed with I/O entries or they may be the only entries used.

Locations 20 through 67 and 5000 through 5777 are reserved for operator use.

Locations 6000 through 6777 are reserved for the input buffer. If no input operation is to be performed, this area may be used to store a program.

Locations 7000 through 7777 are reserved for the output buffer. If no output operation is to be performed, this area may be used to store a program.

Example:

One wishes to read cards from card reader on channel 12, equipment 4, punch the card on card punch channel 12, equipment 5, and output the card on line printer channel 11, equipment 6. Enter the following.

Entry	Description
T	Sets test mode.
RQC12.	Sets up PSX to use channel 12.
CON4000.	Connects card reader.
FNC1.	Sends function 1 to card reader.
INP120.	Inputs one card.
B,IO	Transfers input buffer to output buffer.
CON5000.	Connects card punch.
FNC1.	Sends function 1 to card punch.
OUT120.	Outputs one card.
RLC12.	Releases channel 12 to SMM.
RQC11.	Sets up PSX to use channel 11.
CON6000.	Connects line printer.
OUT104.	Outputs one line (one card).
RLC11.	Releases channel 11 to SMM.
SPACE	Starts program running until S key is depressed.

To use MODE I connect and function, set location 1500-0020. To wait not busy before sending a function to the equipment, set location 1663=XXXX, where XXXX = the wait count in seconds.

Any channel error encountered while doing an I/O operation will be displayed in the standard PSIO format.

If a channel error exists during a run in test mode, start the program over by a G, or space, or continue on by releasing the display to CPC and typing x.GO, where X= PPU that PSX is running in. Set 1501=0001 to ignore channel errors and loop, waiting for an accept, reply, etc. from the controller.

The SCOPE version of PSX operates in the same fashion as the SMM version with the following exceptions.

1. Only the display may be assigned to the control point. D entry will release the display to the system. Any channel error will abort PSX. If peripherals are to be used, they must first be turned off. Also, the entry RQCX. must be used before the program and RLCX. must be the last entry.
2. PSX may be called in by job cards or DIS. No central memory is used.

3. Direct locations 30 through 47 may be used under the system version of PSX.

CPU TEST MODE UTILITY PROGRAM (TST)

DESCRIPTION

TST is an auto mode multiprocessing utility program. When TST is called, it enters a PPU, locks out CPC's CPU control, and begins to repeatedly exchange the CPU selected. It uses the exchange package and program in the CPU that the user sets up before loading TST.

USAGE

The following are commands that the user may use to control TST.

TST,0.cr or TST.cr	This command causes TST to load and begin repeated exchanges to CPU0, using the exchange package at location 400B as the input exchange package address and 420B as the output exchange address.
TST,1.cr	This command causes TST to load and begin repeated exchange to CPU1, using the exchange package at location 600B as the input exchange package address and 620B as the output exchange address.
n.DROP.cr	Where n is the PPU number for TST, this command causes TST to clear CPC lockout, exchange the CPU out, and idle that PPU.
n.STOP.cr	This command causes TST to exchange the CPU out and clear CPC lockout. It then waits for either a go or drop command.
n.GO.cr	This command causes TST to exchange the CPU in.

MESSAGES

SET PARAMS - mm/dd/yy

This message is displayed at parameter stop only. This message must be displayed if the user desires to use the n. DIS. command. The mm/dd/yy represents the month, day, and year of the latest assembly of FAD.

NOTE

Parameter stop results when the commands TST,4. or TST,5. are used.

*** CPU IN TEST MODE ***

This message is present in the CPC message buffer only when TST is repeatedly exchanging. Thus it is a running message.

INPUT PACKAGE = xxx (EXCH ADDRESS = yyy)

This message is displayed at all times in the PPU's message buffer. For CPU0, xxx is 400 and yyy is 420. For CPU1, xxx is 600 and yyy is 620.

NOTE

1. The time between two exchanges is approximately 194 microseconds.
2. The user must load or write into central the CPU program desired.
3. The user must set up the exchange package at 400 or 600 before running TST.

CPU COMMAND TESTS

Mnemonic	Loading Mode	Parameters	Error
ALS/ALX	LDR, Auto, Stand-Alone	None	ALS Stop: P = 224 Start: P = 225 Restart: Set P = 227 ALX Stop: P = 233 Start: Set P = 234 Restart: Set P = 236
BD1/BDP	LDR, Auto, PS for BD1 under SMM and BDP under EXC / CPC	Nonstandard (refer to publication no. 60160600)	Refer to publication no. 60160600

BGK	LDR, Auto, Stand-Alone	None	If (P) = 40, check B1 through B7 = -1 (registers not equal to -1 are failing registers).
			If (P) = 41, check X0 through X7 = -1 (registers not equal to -1 are failing registers).
			If (P) = 42, check A0 through A7 = -1 (registers not equal to -1 are failing registers).

Mnemonic	Loading Mode	Parameters	Error
CMS	LDR, Auto, Stand-Alone	None	Stop (P)=204 First CMU instruction: (P)= 201. Second CMU instruction: (P)=202. CMU history table: (P)= 202-222. Current random number: (P)=227. Initial random starter: (P)=230.
CT1/CTC	LDR, Stand-Alone (CTC may also be called under LDR/CPC)	SSE or CSE: set or clear STOP ON ERROR SSS or CSS: set or clear SECTION STOP SST or CST: set or clear TEST STOP at end of part 1 SSC or CSC: set or clear CONDITION STOP SRS or CRS: set or clear REPEAT SECTION SRT or CRT: set or clear REPEAT TEST, part 1 SRC or CRC: set or clear REPEAT CONDITIONS	

Mnemonic	Loading Mode	Parameters		Error
CT1/CTC (Cont'd)		T: select/release test mode BC: bypass CQL and begin CT1/CTC. SPACE: start test or resume test after stop CPU0 or CPU1: select CPU0 or CPU1 for testing only at start of test		
CT3	LDR, Auto, Stand-Alone	Address 2, A	A=0, use program supplied number. A=X, use X as base for random number.	Answer Difference: ERROR PASS X message is in dayfile checksum difference. CHECKSUM ERROR PASS X message is in dayfile. (For detailed information, refer to publication no. 60160600.)
		Address 3, I	I=0, include CMU instructions (default). I=1, disallow CMU instructions.	
		Address 4, C	Length of random loop (0 through 77B) C= 0, use 5 as length of loop. C=X, use X as length of loop.	

Mnemonic	Loading Mode	Parameters		Error
CT3 (Cont'd)		Address 5, D	D=0, use dump and continue. D=1, use stop. D=2, use loop on failure. D=3, negative. (Refer to publication no. 60160600.)	
		Address 6, E	E=0, use out of stack. E=1, use in stack.	
		Address 7, F	F=0, do not use this option. F=X, use X as pass count.	
		Address 10, G	G=0, do not use optimization. G=1, use optimization.	
		Address 11, H	H=0, use 1 (number of times to test loop before generating new loop). H=X, use X.	
		Address 12, J	J=0, do not use this option.	

Mnemonic	Loading Mode	Parameters	Error
CT3 (Cont'd)		J=1, use only instruction in table (addresses 13B through 46B). J=2, do not use the instruction in the table. Address 13, K K=X, use X as the fm part of the instruction. Address 14, L L=0, do not shorten loop to isolate error. L=1, shorten loop to isolate error. Address 15-46 M=X, use X as the fm part of the instruction.	
CU1	LDR, Auto, Stand-Alone	None	For increment Xj, Bk, Bj, Aj, error stops between 310 and 600. For long add Xj,Xk, error stops between 602 and 743. For multiply Xj,Xk, error stops between 744 and 1067. For divide Xj, Xk, error stops between 1070 and 1247. For floating add Xj, Xk, error stops between 1250 and 1411. For shift Xk, Bj, error stops between 1412 and 1571

Mnemonic	Loading Mode	Parameters	Errors
CU1 (Cont'd)			For boolean Xj, Xk, error stops between 1572 and 1733. For testing X to Q paths, error stops between 1734 and 2014. For testing critical paths Xj, Bk, Bj, error stops between 2015 and 2306. For testing A register critical paths, error stops between 2307 and 2405. For testing B register critical paths, error stops between 2407 and 2475. For testing X register critical paths, error stops between 2477 and 3042. For testing functional units, error stops between 3050 and 5551. (For detailed information, refer to publication no. 60160600.)

Mnemonic	Loading Mode	Parameters	Errors
CU2 (binary only)	LDR, Auto, Stand-Alone	Start test at 00012 Error stop at 002777 Restart at 000012 Address of failing number - X5 Correct number - X3 Failing number - X2 Cycle count - X6	Program displays the address of failure, correct number, and failing number.
CU3 (binary only)	LDR, Auto, Stand-Alone	Breakpoint (P=10) = Normal start. Reloads and runs all phases (P=331) = Abnormal start; does not reload (P=23) = End of pass, checksums have been compared and results are in X7 (P=11) = Convenience stop, allows for breakpoint next at P=10 (P=1373) 0531) = Breaks program into 18 divisions, one division/pair stops	Stops (P=24) = Checksums do not compare (P=1400) = Error found during housekeeping but checksums agree (P=anything else) = Usually a hangup of program

Mnemonic	Loading Mode	Parameters	Errors
CU3 (binary only) (Cont'd)		(P=1425) = Breaks one of 18 divisions into seven subdivisions 1405)	
EJT	Deadstart binary, DSCL binary, ENS, LDR, Auto, Stand-Alone	The following parameters are set by SXX (cr) and cleared by CXX (cr) SE = Stop on errors SS = Stop at end of section RC = Repeat conditions PO = Test central processor 0 66 = Section 4 breakin at 3, 4, 5, and 6 microseconds MC = Central memory conflict SC = Stop on section conditions ST = Stop at end of test RS = Repeat section P1 = Test central processor 1	Messages EXN TOO LONG - EXN is taking too long. EXN TOO SHORT - EXN executed too quickly. EXN HUNG IN PP-1 - PP1 unable to exchange the CP. CENTRAL P ERROR - EXP. P=xxxxxx GOT P=yyyyyy. P+RA ADDER ERROR - Expected result XN=Y. Result got XN=Z. EXCH. PACKAGE ERROR - Error in X (X)=which register miscompares. BREAK-IN ERROR BK-IN PAUSE = N U=SEC EXPECTED RESULT=X RESULT GOT =Y MEM CONFLICT ERR N EXPECTED RESULT=X RESULT GOT =Y

Mnemonic	Loading Mode	Parameters	Error
ERX	LDR, Auto, Stand-Alone	Address 1500=XXX1 Fast mode operation =XXX2 Stop on error =XXX4 Stop at end of section =XXX1 Stop at end of test 1501=1XXX Repeat test =2XXX Repeat section =4XXX Repeat last condition 1502=4XXX ECS present =2XXX CPU speed-up option in =1XXX Do not execute legal ECS instructions =X1XX Low speed CPU	ERROR EXIT TEST Processor X (0 or 1) Pass xxxx Error Mode X (0 or 7) RA=xxxxxx FL=xxxxxx Program=xxxxxxxxxxxxxxxxxxxx Stop Inst 56600000000000000000 X5 xxxxxxxxxxxxxxxxxx X2 xxxxxxxxxxxxxxxxxx X0 xxxxxxxxxxxxxxxxxx X6 xxxxxxxxxxxxxxxxxx A6 xxxxxx (A6) xxxxxxxxxxxxxxxxxx B5 xxxxxx Errors xxxx Loops xxxx P=xxxxxx Exp(RA)=xxxxxxxxxxxxxxxxxx Rec(RA)=xxxxxxxxxxxxxxxxxx Exp CM xxxxxx =xxxxxxxxxxxxxxxxxx Received =xxxxxxxxxxxxxxxxxx xxxxxx Test Errors

Mnemonic	Loading Mode	Parameters		Errors
ERX (Cont'd)		Address 1502 =X2XX	Medium speed CPU	
		=X4XX	High speed CPU	
		1503= XXX1	Single CPU	
		=XXX2	Dual CPU	
		1504=XXX1	Run CPU-0 only	
		=XXX2	Run CPU-1 only	
		=XXX3	Run both CPUs	
		1505	Not used	
		1506	Not used	
		1507=0000	Run constant address of RA	
		=00RR-RR	Upper six bits of RA; do not use RA	

Mnemonic	Loading Mode	Parameters			Errors
ERX (Cont'd)		Address	1510=0000	Run constant update of RA	
			=RRRR	Use RRRR for lower 12 bits of RA; do not update RA	
			1511=0016	Section select bits (bit 1 = section 1, etc)	
			1512=XXXX	CPU type in display code (preset by ERX)	
			1513=0BBB	Number of banks of CM (preset by ERX)	

Mnemonic	Loading Mode	Parameters	Error
FDT	LDR, Auto, Stand-Alone	None	Hangs in error loop upon detection of failure register date at time of error: (X1) = Random operand, OP1 (X2) = Random operand, OP2 (X3) = Divide unit answer (X4) = Simulated answer (X5) = Error difference The DIV-SIM data map begins at location 200: (200) = XJ (dividend) (201) = XK (divisor) (203) = Simulated quotient, no exponent (204) = XI (quotient from divide unit) (206) = 1X pick value (207) = 2X pick value (210) = 3X pick value (212) = Original value
FM1	LDR, Auto, Stand-Alone	Backspace and then hit spacebar to restart after error.	Memory data while in error loop: (50) = Unit 1 answer of X1*X2 (51) = Unit 2 answer of X1*X2 (52) = Unit 1 answer of X2*X1 (53) = Unit 2 answer of X2*X1 (54) = Unit 1 and 2 difference data for X1*X2 (55) = Unit 1 and 2 difference data for X2*X1

Mnemonic	Loading Mode	Parameters	Errors
FM2	LDR, Auto, Stand-Alone	Backspace and then hit spacebar to restart after error.	Memory data while in error loop: (70) = Unit 1 answer of X1*X2 (71) = Unit 2 answer of X1*X2 (72) = Unit 1 answer of X2*X1 (73) = Unit 2 answer of X2*X1 (74) = X1*X2 unit difference data (75) = X2*X1 unit difference data
FST	LDR, Auto, Stand-Alone	Failing fast loop starts at 260 Slow loop starts at 441 Slow loop answers at 310 Fast loop answers at 330 Slow loop results of last error at 350 Fast loop results of last error at 370 Compare difference at 300 Slow loop result at 301 Fast loop result at 302 Address slow loop result 303 Address fast loop result 304 Error count 305 Pass count 306 Repeat flag 307	Program halts with P=213 when an answer difference occurs between the slow and fast loops. If program halts with P=213 (not legitimate error), run another program.

Mnemonic	Loading Mode	Parameters	Errors
IMC	LDR, Auto, Stand-Alone	Address 000002 = XXX1 Repeat test section = XXX2 Repeat last error condition = XXX4 Suppress error reports = XX1X Stop at end of section = XX2X Stop on error = XX4X Stop at end of test = X1XX Loop on error = X2XX Repeat test = X4XX Display running message 000003 = SSS1 Section 0 - Floating 40 check = SSS2 Section 1 - Floating 41 check	Display Format IMC Test Error Stop Section S Error Code YY (S = test section and YY = message code) Data 1 - Unit 1 product of X1*X2 Data 2 - Unit 2 product of X1*X2 Data 3 - Unit 1 product of X2*X1 Data 4 - Unit 2 product of X2*X1 Data 5 - Simulated product Data 6 - Instruction stack Data 7 - X1 operand Data 8 - X2 operand (Also located in addresses 10 through 17.)

Mnemonic	Loading Mode	Parameters		Errors
IMC (Cont'd)		Address 000003 = SSS4	Section 2 - Floating 42 check	
		= SS1S	Section 3 - Integer times floating check	
		= SS2S	Section 4 - Floating times integer check	
		= SS4S	Section 5 - Positive integer times positive integer check	
		= S1SS	Section 6 - Negative integer times negative integer check	
		= S2SS	Section 7 - Negative integer times positive integer check	

Mnemonic	Loading Mode	Parameters	Errors
IMC (Cont'd)		Address 000003 = S4SS Section 10 - Positive integer times negative integer check = 1SSS Section 11 - Random integer check 000004 = XJ operand 000005 = XK operand 000006 = Records total number of errors during test execution	

Mnemonic	Loading Mode	Parameters	Errors
IWS	LDR, Auto, Stand-Alone	None	Section 1 Error Stops Register Stop(1) Stop(2) X0 42 130 X1 45 133 X2 47 135 X3 51 137 X4 53 141 X5 55 143 X6 57 145 X7 61 147 B2 63 151 B3 65 153 B4 67 155 B5 71 157 B6 73 161 B7 75 163 Section 2 Error Stops (P) - 247 Stack contents at addresses 236 through 245 (P) - 264 Stack contents at addresses 153 through 261

Mnemonic	Loading Mode	Parameters	Errors
IWS (Cont'd)			Section 3 Error Stops Stops anywhere in stack Stack contents at addresses 324 through 333 Section 4 Error Stops (P) - 365 Stack contents at addresses 354 through 363 (P) - 401 Stack contents at addresses 370 through 377
LAT	LDR, Auto, Stand-Alone	Backspace and then hit spacebar to restart after error.	When an error occurs, the test will hang in a loop upon an error. The following information applies. (X1) = Random operand, OP1 (X2) = Random operand, OP2 (X3) = The unit answer (hardware) (X4) = Simulated answer (X5) = Logical difference data

Mnemonic	Loading Mode	Parameters	Errors
MAN	LDR, Auto	Address 1500=XXX1 Repeat subcondition =XXX2 Stop on error =XXX4 Stop at end of section =XX1X Stop at end of test =XX2X 6681 mode I (not used) =XX4X Stop at end of pass =X1XX Stop at end of condition 1501=XXX1 Delete running message =XXX4 Print errors =XX1X Bypass error message =XX2X Drop CLK when dropping MAN =XX4X Drop CMC when dropping MAN =X4XX Repeat pass =1XXX Repeat test =2XXX Repeat section =4XXX Repeat condition =4X11 Tight loop desired 1502=4137 6400 type of CPU =4140 6500 type of CPU =4141 6600 type of CPU =4142 6700 type of CPU	Due to the number of errors (12 pages of error codes) and the error format explanation, refer to all the error code descriptions in publication no. 60160600.

Mnemonic	Loading Mode	Parameters	Errors
MAN (Cont'd)		Address 1502=4235 72XY type of CPU =4236 73XY type of CPU =4237 74XY type of CPU 1503=0000 One CPU =0001 Two CPUs 1504=XXX1 MAN instruction (262X) present =XXX2 Interrupt and mask register present =XXX4 ECS registers present =XX1X Use exit mode register set =XX2X 32K CM available =XX4X 00 exchange JP, exchange on HLT, and error exit present =X1XX P+2 speedup present (6600 only) =X2XX Illegal instruction exit present (6600 only) 1505 - Not used 1506 - Not used 1507 - Section flags corresponding to locations 1526 through 1541 of section selection register	

Mnemonic	Loading Mode	Parameters	Errors
MAN (Cont'd)		Address 1510 - Section flags corresponding to locations 1512 through 1525 of section selection register 1511=XXX1 Pass 0, CPU-0 test, all CMCs stopped =XXX2 Pass 1, CPU-0 test, all CMMs running =XXX4 Pass 2, CPU-1 test, all CMCs stopped =XX1X Pass 3, CPU-1 test, all CMCs running 1512 - Section selection register 1541 used by variable distributor	
MXJ	LDR, Auto, Stand-Alone	All test parameters are keyboard entries of the form $X_1X_2X_3$ (cr) X1=S (set), R (release), or C (clear) X2, X3=Actual parameter or section number SES or RES or CES = Error stop SCS + RCS + CCS = Condition stop SSS + RSS + CSS = Section stop SPS + RPS + CPS = Pass stop STS + RTS + CTS = End of test stop SRT + RRT + CRT = Repeat test	Messages 2610 execution-MF=1 013 execution-MF=1 2610 execution-MF=0 013 execution-MF=0 CR-1 TR-0 CR-0 TR-1

Mnemonic	Loading Mode	Parameters	Errors
MXJ (Cont'd)		SRP+RRP+CRP = Repeat pass SRS+RRS+CRS = Repeat section SRC+RRC+CRC = Repeat condition SYY+RYY+CYY = Select or deselect section YY SA+RA+CA = Select or deselect all sections PPU Parameters PPXXXX(cr), where XXXX is a 12-bit code defined as follows: 4000 Central write (one word unless block transfer bit set) 2000 Central read (one word unless block transfer bit set) 1000 Block transfer (five words with read and/or write) 0400 Loop with (A) register=777777B 0200 Clear loop on current buffer pattern 0100 Delay between read and write 0040 Select loop on current buffer pattern 0037 PPU/channel number 0015 Turn all PPUs on simultaneously 0014 Turn all PPUs off simultaneously	WWWW address-XXXX (WWWW = type of exchange and XXXX = source of exchange address.) CR-YYYYYY (intended address) TR-ZZZZZZ (improper address) Exchange data CR-YYYY YYYY YYYY YYYY YYYY TR-ZZZZ ZZZZ ZZZZ ZZZZ ZZZZ No 2610 abort on 013

Mnemonic	Loading Mode	Parameters	Errors
MXJ (Cont'd)		00NN Turn off PPU NN (loop with a register=0) MMNN PPU NN continues reads and writes with data pattern MM	
POP	LDR, Auto, Stand-Alone	Backspace and then hit spacebar to restart program.	Hangs in loop on error (memory data while in error loop) Location 50 = Failing test number 51 = Hardware population count 52 = Simulated population count 53 = Logical difference error data

Mnemonic	Loading Mode	Parameters	Errors
RAN	LDR, Auto, Stand-Alone	None	Error halt = 567 Fast failing loop starts = 402 Slow loop answer = 1000 Register results before execution of last instruction = 1040 Pass number = 266 Compare difference = 260 Fast loop result = 261 Failing register = 263 Slow loop starts at = 615 Fast loop answer = 1020 Error count = 265 Slow loop result = 262 Fast loop pass count = 232
RTJ	LDR, Auto, Stand-Alone	Ao defines the upper limit of the return jump array.	The program will stop on an error. The difference between B3 and B5 indicates the error data. (B3) holds the computer jump value. (B5) holds the return jump value.
RX7	LDR, Auto, Stand-Alone	None	Error occurred if P stops cycling.

Mnemonic	Loading Mode	Parameters	Errors
STC	LDR, Auto, Stand-Alone (valid on 6600 only)	Address 1736=000-000 (disables 1 display option)	Messages Failure in stack at I 000003 Failing instruction 20201460004600046000 Address plus one of failing loop 0000501 Failure in parcel 0------0 Example: ****Register Contents at Time of Failure**** BO=000000 X0=00------00 B1 =000000 X1=00------00 B2 =0000214777 X2=00------01 B3 =0000000501 X3=00-------0 B4 =0000000000 X4=00-------0 B5 =0000000002 X5=00-------0 B6 =0000000010 X6=00-------0 B7 =0000000003 X7=00-------0 **** Correct Register Contents **** B0 =00------00 X0=00------00 B1 =Pass count X1=00------00 B2 =00------00 X2=00------02 B3 =Address of stack entry X3=00------00 B4 =Failing parcel X4=00------00 B5 =Failing test section X5=00------00 B6 =Failing X register X6=00------00 B7 =Failing I register X7=00------00

Mnemonic	Loading Mode	Parameters	Errors
STK	LDR, Auto, Stand-Alone	Starting address is 000003. To restart, set P=277, breakpoint at 300, set P=17, and run. Address 3000 is restart or continue address (may be changed to jump to another program).	If error occurs, program jumps out of stack and halts on a 00 instruction.
TOC	LDR, Auto, Stand-Alone (only valid on 6600, 6600 head of 6700, and CYBER 74)	Space to start and backspace 70 to stop.	Error stop with (P)=317. Failing test case is in locations 134 through 137. Input/output packages are at locations 200 through 237 in exchange package format.

CENTRAL MEMORY TESTS

Mnemonic	Loading Mode	Parameters	Errors
CM6	LDR, Auto Stand-Alone	To restart after error: ENX1.0. (cr) ENP,341.(cr) Space	LOC,342 Failing CM address LOC,343 Contents of failing address LOC,344 Pass counter LOC,345 Number of passes test is to run before restarting LOC,346 Number of instack read loops to be made on an address P=340 Normal error stop P=Anything else Usually a CP timing hangup.
CSC	Stand-Alone, ENS, LDR SECDED switch in SECDED or PARITY position.	Address 1500=XXX2 Stop on error XX1X Stop at end of test XX2X Abort error checking 1501=1XXX Repeat test 2XXX Repeat section (same bank and quad)	Errors are indicated by self-explanatory messages that appear on the display screen.

Mnemonic	Loading Mode	Parameters			Errors
CSC (Cont'd)		Address	1502=XXX4	CPU is model 175	
			XX1X	Test CSU 0	
			XX2X	Test CSU 1	
			1503=0XXX	Number of 4K increments in central memory	
			1504=XXX0	PPS 0 PPUs to sweep central memory (PPUs 0, 1, and 2 are unavailable and will be ignored if selected); bit 3 selects PP 3, etc.	
			1505=XXXX	PPS 1 PPUs to sweep central memory; bit 0 selects PP 20, etc.	

Mnemonic	Loading Mode	Parameters			Errors
CSC (Cont'd)		Address	1510=XXXX	Sections: bit 0=section 0, etc.	
			1513=CCOE	Printer channel and equipment (if zero, printer output is deselected)	
			1514=0XXX	Banks: bit 0= bank 0, etc.	
			1515=XXXX	Quads: bit 0= quad 0, etc. (if zero, test all quads in the system)	
			1516=XXXX	Section 2 write count	
			1517=XXX1	Stop on each data error	
			XXX2	Delete end test printout	
			1520=XXX1	Display all single SEC-DED errors	

Mnemonic	Loading Mode	Parameters		Errors
CSC (Cont'd)		Address 1520 = XXX2	Stop and display all single SECDED errors	
		XX1X	Display all double SEC-DED errors	
		XX2X	Stop and display all double SECDED errors	
		4XXX	Read and display chip selection error	
		1521=XXX0	Run slow mode sections	
		XXX1	Run fast mode sections	
		1522=00XX	Pattern selection, four possible combinations to test CS and CU modes	

Mnemonic	Loading Mode	Parameters	Errors
CSC (Cont'd)		Address 1523 and 1524= 00XXXXXX PP sweep area, lower limit 1525 and 1526= 00XXXXXX PP sweep area, upper limit 1527=XXX0 Do not use CPU 1 (C174) XXX1 Use CPU 1 to sweep (C174)	
MM1, M1R, M1A, M1B, M1C, M3C, MM4, MM3, M3R, M3A, and M3B	LDR, Stand-Alone (Auto for MM4 only)	MM1, M1R, M1A, and M1B test central memory from the CPU. MM1 is the basic test. M1R has all the PPUs doing phased reads of central memory. M1A is the equivalent of MM1 and M1B is the 32K equivalent of M1R. Use M1C and M3C for 49K or 98K. Use MM4 under auto.	

Mnemonic	Loading Mode	Parameters	Errors
MM1 etc. (Cont'd)		MM3, M3R, M3A, and M3B are the same as MM1 through M1B, except they are more rigorous and lengthy. MM3, M3R, MM1, M1B, M1R, M1A, and MM4 will run in CPU-0 or CPU-1. Keyboard Entries SE Stop on error SP Stop at end of pattern RP Repeat current pattern SB Stop at end of bank RB Repeat current bank ST Stop at end of test CXX Clear the above selections BK Add banks to be tested CBK Delete banks BK8 Sets all banks to be tested SPACE Continue test / Return to PS (To restart the test, do a 0221X1000. To return to where the test was, do a 0221W2060.) AB Terminates testing of current bank and goes to next bank	

Mnemonic	Loading Mode	Parameters	Errors
MM1 etc. (Cont'd)		Left Scope Displays Bank — Current bank being tested Pass — Number of passes for current bank Bit — Bit numbers 0 through 59 (0 through 11 leftmost module) Number of errors — Octal count of cumulative errors Common add bits — Mask showing which address bits have been the same for all errors on the plane Last address — The address at which the last error occurred for each bit (the address within the bank) Correct bit — 1 = dropping the bit and 0 = picking the bit	

Mnemonic	Loading Mode	Parameters	Errors
MM2 and M2U	Deadstart Binary, DSCL Binary, ENS, Stand-Alone, LDR	Test displays the operating instructions. Type the following for desired testing. L Run all tests Z Zeros and ones R Random pattern CR Display PP memory F Full address W Worst pattern B Select one bank SPACE Continue S Stack address C Checkerboard pattern U Select upper bank / Restart	Display 1. Pass count 2. Section and cycle being run (complement, up or down) 3. Chassis and bank being tested 4. Errors, if any Error Format Address Contents of Failing Location XXXXXX YYYY YYYY YYYY YYYY YYYY
MMX	Deadstart Binary, DSCL Binary, ENS, Stand-Alone, LDR	MMX is a stand-alone CYBER 170 PPU-based test of central memory.	Errors are listed in an error display and are announced by error messages, which are self-explanatory.

Mnemonic	Loading Mode	Parameters			Errors
MMX (Cont'd)		Location	Default	Description	
		3	XXXX	Number of PPUs in system.	
		4	0000	Memory size in 4K blocks.	
		5	1457	Status/control register word zero bits to be tested for error and message to be displayed.	
		6	1100	Control flags: XX2X = Stop in individual error XX4X = Stop on end of section X1XX = Stop at beginning and end of test 1XXX = Stop on error buffer full	
		7	0174	Section flags 0 through 6	
		10	1375	PP enable bits, PPS0.	

Mnemonic	Loading Mode	Parameters			Errors
MMX (Cont'd)		Location	Default	Description	
		11	XXXX	PP enable bits, PPS1.	
		12	XXXX	CSU selected for test.	
		13	XXXX	CSU 0 quads selected to test.	
		14	XXXX	CSU 1 quads selected to test.	
		15	0377	Banks selected to test.	
		16	0	Nonzero aborts data error checking by the slave PPs to speed the running of the test.	
		17	0	Nonzero aborts pre-section read to verify data retention.	
		75	0	Nonzero if chip is logged in SCR on SECDED error (ECO CA 37767).	
		Keyboard Commands			
		The following one-word commands act as a restart of the test with the specified			

Mnemonic	Loading Mode	Parameters	Errors
MMX (Cont'd)		parameter changed; all other parameters remain the same. L — Run all standard default selected section L, XXXX — Run sections XXXX Z — Run zeros section (section 0) 0 — Run ones section (section 1) M — Run march section (section 2) P — Run march with SECDED patterns (section 3) F — Run full address section (section 4) A — Run chip addressing section (section 5) R — Run random section (section 6) Q, X — Test quad X Q, X, Y — Test quad X through Y C, X — Test CSU X C, X, Y — Test CSU X and Y B, X — Test bank X B, X, Y — Test bank X through Y	

Mnemonic	Loading Mode	Parameters	Errors
MMX (Cont'd)		Scoping Commands The following commands are for scoping purposes and are functional only when the test is stopped. RWA X, YYYYYY, ZZZZ, ZZZZ, ... ZZZZ — Read and write address YYYY with pattern ZZZ, ZZZ using PPU X. ROA X, YYYYYY — Read one location YYYYYY using PPU X. WOA X, YYYYYY, ZZZZ, ZZZZ, ... ZZ — Write one address YYYYYY with pattern ZZZ...ZZZZ using PPU X. General Test Control Commands / — Restart the test and reset all parameters to their default values. I — Ignore errors, errors not displayed on left screen, or errors indicated by error counters.	

Mnemonic	Loading Mode	Parameters		Errors
MMX (Cont'd)		SPACEBAR	Start the test. If the test is stopped by backspace, continue.	
		BACKSPACE	Stop the test.	
		RDS	Display the running display on the right screen.	
		PPXX, FWA	Select PP XX for PP memory display on right screen.	
		DIX, YYYY	Change the starting address of PP memory display in block X to address YYYY.	
		+	Increment each PPU memory display block FWA on the right screen by 100B.	
		-	Decrement PP memory display address on right screen as for + entry.	
		BN	Null display right screen.	
		EPX, YYYY, Z1, Z2, Z3, Z4, Z5	Enter address YYYY with ZZZZ in PP memory X. If X is zero, actual address will be changed. If X is nonzero, the	

Mnemonic	Loading Mode	Parameters		Errors
MMX (Cont'd)			address relative to the start of slave program stored in PP0 memory will be changed. The PPU must be reloaded using the MP command.	
		YYYY, Z1, Z2, Z3, Z4, Z5	Enter up to five bytes of data in PP0 memory starting with address YYYY.	
		SCR, X	Display status/control register X on right screen; command is ignored if there is only one SCR.	
		CE	Clear all errors in SCR.	
		CB2X	Clear/set PPU 2X speed in SCR.	
		SC2X		
		CB, XXX, Y	Clear/set bit XXX in status/control register Y. If Y is not specified, SCR 0 is assumed.	
		SB, XXX, Y		
		MP X	Reload slave program into PPU X. Test must be stopped when this command is entered.	

Mnemonic	Loading Mode	Parameters	Errors
MMX (Cont'd)		DP X — Deadstart PPU X.and restart the program executing at address 100B. **NOTE** If X is omitted on MP or DP command, all slave PPUs selected in parameters 10 and 11 will be loaded or deadstarted. DS X — Set PP X in the PPU select bits in the corresponding status/control register. Set the PP select mode bit.	
M2C (49K or 98K peripheral processor test of CM)	Deadstart Binary, DSCL Binary, Stand-Alone	Enter 0 for 49K and enter SPACE for 98K. 1. (cr), test exits to PP memory display. 2. Left screen will display executable options. 3. To restart test, set 0221 to 1000.	Same as MM2, except for 49K or 98K machine.

Mnemonic	Loading Mode	Parameters	Errors
MY1	LDR, Auto, Stand-Alone	A0 is set to the field length and defines the upper limit.	In the event of error, P=132 At error stop (X7) = holds accumulation of error bits and XX2-X5 should match X0, either in the true or complemented form. If no error is indicated in X1-X5, the error occurred in X1 and was lost when the accumulation check read was done. In this case, the error bits in X7 equal the error bits that occurred in the first X1 read.

Mnemonic	Loading Mode	Parameters	Errors
M65/M98 M65 runs only on machines having 32K, 65K, or 131K M98 runs on machines having 49K or 98K (PPUs 0, 1, 10, and 11 must be available.)	LDR, Stand-Alone	The following entries are used. **NOTE** M98 has no section 7. Test Section TSXX Add section XX to list of selected test sections CTSXX Clear section XX from list of selected test sections TSA, TS8 Select all test sections CTSA CTS8 Deselect all test sections **NOTE** After a TSXX or CTSXX, enter only XX to select or deselect section XX. Bank Selection BKXX Add bank XX to the list of selected banks CBKXX Remove bank XX from list of selected banks	Display Left Screen Bit in error Number of errors in the current bank Common address bits Last failing address Correct bit Display Right Screen Test title Number of banks Central processor selection Current P0 and P1 Current bank, pass section, and pattern Test status (type of stop encountered or current test address) Selected options Selected test section Selected PPUs Selected banks to be tested

Mnemonic	Loading Mode	Parameters	Errors
M65/M98 (Cont'd)		Bank Selection (Cont'd) BKA Select all banks BK8 CBKA, Deselect all banks CBK8 **NOTE** After a BKXX or CBKXX, enter only XX to select or deselect bank XX. PPU Selection PPXX Add PP-XX to list of selected PPUs CPPXX Remove PP-XX from list PPA or Select all PPUs PP8 CPPA Deselect all PPUs or CPP8 SE Stop on error SP Stop at end of pattern RE Record errors on 501 (1002-CCEE)	

Mnemonic	Loading Mode	Parameters	Errors
M65/M98 (Cont'd)		PPU Selection (Cont'd) SS Stop at end of test section SB Stop at end of bank ST Stop at end of test RP Repeat pattern RS Repeat section RB Repeat bank RT Repeat test CXX Clear XX selection (any of the above 10 selections) Monitor Control SPACE Continue test after any test stop. CARRIAGE RETURN Exit from monitor to PP1 PS or exit from PS to monitor. = Exit to PP0 PS or return to monitor from PP0 PS. / Restart the test with standard test parameter selections. * Exit from monitor to central memory display or return.	

Mnemonic	Loading Mode	Parameters	Errors
M65/98 (Cont'd)		Central Processor Selection The following are entered at the start of the test. CPU — No central processor is selected (used for section 7 only) CPU0 — Central processor 0 only CPU1 — Central processor 1 only CPU01 — Central processor 0 is the control processor; Central processor 1 is the slave processor CPU10 — Central processor 1 is the control processor; Central processor 0 is the slave processor	

PPU TESTS

Mnemonic	Loading Mode	Parameters	Errors
CED (Modified PC1)	Deadstart under DS panel control	None	Hangs on failing instruction. Consult listing of CED to identify failure. Refer to CED description.
CHT	Deadstart Binary, DSCL Binary, ENS, Stand-Alone	Address 1001=Nonzero. PP0 will check all channels operating properly and loop under normal PS display for section 1 run. 1002=AABB. Check two PPs that may be suspect AA=PPA or output PP BB=PPB or input PP 1003=OOCC, channel number for AA and BB to test	Messages ERR MES+0 Disconnect CHXX — Channel XX should have been deactivated, but was active. ERR MES+1 IJM CH INAC CHXX — Channel XX is inactive but no jump occurred on IJM. ERR MES+2 AJM CH INACT CHXX — Channel XX is inactive but no jump occurred on AJM. ERR MES+3 AJM CH ACT CHXX — Channel XX is active but no jump occurred on AJM.

Mnemonic	Loading Mode	Parameters	Errors	
CHT (Cont'd)		Address 1004=Number of words PPA will transmit to PPB, normally 5000g, unless changed (must be 5000g) Space Bar =Start S Key =Stop * =Return to PS display	ERR MES+4 Activate CHXX	Channel XX should have been activated but was deactive.
			ERR MES+5 JM CH full CHXX	Channel XX is full but no jump occurred on FJM.
			ERR MES+6 ORN failed CHXX	Channel XX failed to output from a register (PP0).
			ERR MES+7 EJM CH Empt CHXX	Channel XX is empty but no jump occurred on EJM.
			ERR MES+10 IAN Failed CHXX	Channel XX failed to input to a register (PP0).
			ERR MES+11 PPXX not idle DS	PPX is not idled; requires deadstart.

Mnemonic	Loading Mode	Parameters	Errors	
CHT (Cont'd)			ERR MES+12 ILLEGAL PP	Address 1002 has a number other than 1 through 11.
			ERR MES+13 ILLEGAL CHANNEL	Address 1003 has a number other than 1 through 13.
			ERR MES+14 Space to Start	Normal start message
			ERR MES+15 IJM CH ACT CHXX	Channel XX is active but jump occurred on IJM.
			ERR MES+16 EJM CH FULL CHXX	Channel XX is full but jump occurred on EJM.
			ERR MES+17 FJM CH EMPT CHXX	Channel XX is empty but jump occurred on FJM.
			ERR MES+20 CH INACT CHXX	Channel XX should have been active but was inactive.

Mnemonic	Loading Mode	Parameters	Errors	
CHT (Cont'd)			ERR MES+21 CH FULL CHXX	Channel XX should have been empty but was full.
			ERR MES+22 NEWWWWT=YYYY CHXX	Channel XX did not complete input to a register in time [W= time expected (octal), Y=time received (octal)] .
			ERR MES+23 NEW WWWB= YYYY CHXX	Channel XX did not input data to a register correctly. [W=data expected (octal), Y= data received (octal)].
			ERR MES+24 NEWWWWT= YYYY CHXX	Channel XX did not complete input to memory in time.
			ERR MES+25 MEWWWWB= YYYY CHXX	Channel XX did not input data to memory correctly. W and Y are the same as error message 23.

Mnemonic	Loading Mode	Parameters	Errors	
CH1	Deadstart Binary, DSCL Binary Deck, ENS, Stand-Alone	Address 1001=Nonzero, PP0 will loop checking all channels (section 1) 1003=OOCC, channel number for AA and BB to test 1004=Word count for AA and BB to use (must be 2400_8) S Key =Stop Space =Start * =Return to PS display.	Messages ERR MES+0 Disconnect CHXX ERR MES+1 IJM CH INAC CHXX ERR MES+2 AJM CH ACT CHXX ERR MES+3 AJM CH ACT CHXX ERR MES+4 Activate CHXX ERR MES+5 FJM CH FULL CHXX	 Channel XX should have been deactivated but was active. Channel XX is inactive but no jump occurred on IJM. Channel XX is inactive but jump occurred on AJM. Channel XX is active but no jump occurred on AJM. Channel XX should have been activated but was deactive. Channel XX is full but no jump occurred on FJM.

Mnemonic	Loading Mode	Parameters	Errors	
CH1 (Cont'd)			ERR MES+6 OAN FAILED CHXX	Channel XX failed to output from A register (PP0).
			ERR MES+7 EJM CH EMPT CHXX	Channel XX is empty but no jump occurred on EJM.
			ERR MES+10 IAN FAILED CHXX	Channel XX failed to input to A register. (PP0).
			ERR MES+15 IJM CH ACT CHXX	Channel XX is active but jump occurred on IJM.
			ERR MES+16 EJM CH FULL CHXX	Channel XX is full but jump occurred on EJM.
			ERR MES+17 FJM CH EMPT CHXX	Channel XX is empty but jump occurred on FJM.

Mnemonic	Loading Mode	Parameters	Errors	
CH1 (Cont'd)			ERR MES+20 CH INACT CHXX	Channel XX should have been active but was inactive.
			ERR MES+21 CH FULL CHXX	Channel XX should have been empty but was full.
			ERR MES+22 NEWWWWT = YYYYCHXX	Channel XX did not complete input to a register in time (W= time expected, Y= time received).
			ERR MES+23 NEWWWWB = YYYYCHXX	Channel XX did not input data to A register correctly (W=data expected, Y= data received).
			ERR MES+24 MEWWWWT = YYYYCHXX	Channel XX did not complete input to memory in time (W=time expected, Y=time received).

Mnemonic	Loading Mode	Parameters	Errors
CH1 (Cont'd)			ERR MES+25 MEXXXXB = YYYYCHXX' — Channel XX did not input to memory correctly (W=data expected, Y=data received). ERR MES+ 26 PP NOT 1DLE — Indicates the PP is hung. ERR MES+27 CH EMPTY — Channel should be full but is empty.
CH2	Deadstart Binary, DSCL Binary Deck, ENS, Stand-Alone	Location 1000 Bit 0 Report all errors detected within a block. (If bit 0 is not set, report only the first error.) Bit 1 Stop on error if bit 1=1. Location 1001 Not a parameter, holds the PPU number currently displaying at memory.	Running Message: Word = WWWW A = aaaa E = eeee WWWW = Word number of failure aaaa = Actual data received eeee = Data sent (expected)

Mnemonic	Loading Mode	Parameters	Errors
CH2 (Cont'd)		Location 1002 - Test selection Bit 0 Test PPUs 0 through 9 over channels 0 through 4. Bit 1 Test PPUs 0 through 9 over channels 0, 1, 24 through 33. Bit 2 Test PPUs 0 through 9, 10 through 19 over channels 0 through 4, 20 through 23.	
CHX	Absolute Binary, COMPASS Binary, ENS, LDR Channel parity switches must be on for all enabled channels to run sections 5 and 13 correctly.	CHX is a stand-alone, CYBER 170 channel test. Address 1005≠0000 Delete test module load on repeat condition (scope mode). Address 1006=Control flags =XXX1 Repeat condition =XXX4 Repeat section =XX1X Repeat test =XX2X Stop on error =XX4X Stop at end of section	Errors are revealed through self-explanatory messages that appear at the bottom of the left screen running display. Keyboard Commands CE Clear all error bits in the SCR. Clear/set bits in parameter word 6 (1006): CCS, SCS Stop on condition CES, SES Stop on error CSS, SSS Stop on end of section CTS, STS Stop at beginning and end of test CPS, SPS Stop on channel parity

Mnemonic	Loading Mode	Parameters	Errors
CHX (Cont'd)		=X1XX Stop at beginning and end of test =X4XX Stop at end of each condition =1XXX Stop on channel parity errors Address 1007=Section flags 0 through 11 1010=Section flags 12 through 19 1011=PPU enable bits (PPUs 0 through 11B) 1012=PPU enable bits (PPUs 20B through 31B) 1013=Channel enable bits (channels 0 through 13B) 1014=Channel enable bits (channels 20B through 33B) 1015=Initial data pattern used in sections 7, 15, 17, and 18. 1016=Block length used in sections 7, 15, 17, and 18.	CRC, SRC Repeat condition CRS, SRS Repeat section CRT, SRT Repeat test DIX, YYY Change address of monitor PPU memory display block X to YYYY. DT Display current test module. ET, XXXX, YYYY Enter current test module with data YYYY at address XXXX. EPO, XXXX, YYYY Enter data YYYY into master PPU memory address XXXX. RST Restart the test. AN, BN Toggle A or B display to disable or enable display page. space bar Start the test. cr Stop the test. + Roll memory display forward. - Roll memory display backward.

Mnemonic	Loading Mode	Parameters	Errors
CHX (Cont'd)		Address 1017=Maximum block length mask used in sections 8, 16, and 19. 1020=Minimum block used in sections 8, 16, and 19. 1021=Number of PPUs in system. 1022=Pass count/random seed initial value. 1023=PPS memory type. Bits 0 and 1 are set to show PPS 0 or 1 with 2102 memory.	
1P1	Deadstart Binary, DSCL, Binary Deck, ENS, Stand-Alone	1. Enter W-X-Y-Z carriage return or spacebar only. 2. W determines central memory instruction parameter. (A c will cause them to be tested and n will cause them to be bypassed.) 3. X determines which processor the long test is to be run in. 1 = Processor 1 2 = Processor 2 4. Y determines operands to be used for PP0's test. z = Zeros o = Ones	Test Screen Message Indicates PP and instruction being performed when error occurred.

Mnemonic	Loading Mode	Parameters	Errors
IP1 (Cont'd)		5. Z determines which chassis the test will be run if 20 processors are available. 0 = Chassis containing processors 0 through 10 1 = Chassis containing processors 20 through 30 6. Spacebar, run test with above selected options. Message: Type WXYZ CR W = C or N X = 1 or 2 Y = o or z Z = 0 or 1	
IRT	LDR, Auto	Address 1500=XXX1 Repeat subcondition (ignored in section 12) =XXX2 Stop on error =XXX4 Stop at end of section =XX1X Stop at end of test 1501=1XXX Repeat test =2XXX Repeat section =4XXX Repeat condition	Messages All error messages are prefixed with IRT SXXYY EWW HVVVV XX = Section number WW = Error code YY = Subsection number VVVV = Pointer for the history table Error Code (1) INACTIVE XXXX The interlock channel is [illegible]ctive. XXX[illegible]s

Mnemonic	Loading Mode	Parameters	Errors
IRT (Cont'd)		Address 1501=XXX1 Omit running display =XXX2 Speed up option =XXX4 Send errors to SMM dayfile 1507=Section flags (sections 15B through 30B), bit 0 = section 15, etc. 1510=Section flags (sections 1 through 14B), bit 0 = section 1, etc. 1512=Length of interlock register in bits (100B or 200B) 1515=Number of first slave PPU (used in section 12 only) 1516=Number of second slave PPU (used in section 12 only) **NOTE** The interlock channel number is not parameter selectable. It is assumed that it will always be 15B.	the last instruction code sent to it. Error Code (2) FULL XXXX YYYY The interlock channel is full when it should be empty. XXXX = Last instruction code sent to the interlock register YYYY = Last status word received Error Code (3) EMPTY XXXX The interlock channel is empty when it should be full. XXXX = Last instruction word sent Error Code (4) STATUS AXXXX EYYYY IZZZZ Interlock register failed to return the correct status word. XXXX = Status word returned from the interlock register

Mnemonic	Loading Mode	Parameters		Errors	
IRT (Cont'd)		SPACE	=Continue after stop (unless at the auto display), and type X.60 to restart, where X=PPU number. Type R to restart test completely. Type S to stop program (unless at the auto display), and then type X. Stop.		YYYY = Status word that was expected ZZZZ = Last instruction code that was sent
				Error Code (5) SLOW CHANNEL XXXX	Tried to perform 10,000 interlock register operations apiece from each of two PPs. Timing indicates the interlock channel(s) failed to respond at the expected rate. XXXX = Approximate time in milliseconds to complete the above operations. [If the two PPs are on the same barrel (10 or fewer PPs),

Mnemonic	Loading Mode	Parameters		Errors
IRT (Cont'd)				Error Code (5) (Cont'd) the time should be approximately 60 milliseconds. If the two PPs are on opposite barrels (14 or more PP systems), the series of operations should have finished in about 40 milliseconds.]
MAP	Deadstart Binary, DSCL Binary deck, ENC, Stand-Alone.	Address 1500=XXX1	Compare times of PP-CM instructions against a fixed time	Messages All error messages have the following format. PPX - MMMM XXXX YYYY MMMM - One of the following. CWD PPX is doing only CWD instructions.
		=XXX2	Stop on error, data, or timing	
		=XXX4	Stop at end of section	

Mnemonic	Loading Mode	Parameters	Errors
MAP (Cont'd)		Address 1500=XX1X Stop at end of test =XX2X Stop after each block of test instructions 1501=1XXX Repeat test =2XXX Repeat section =4XXX Repeat condition 1502=1777 All 10 processors selected to reference CM =XXX1 Select PP0 =XXX2 Select PP1 etc. **NOTE** PP0 should always be selected. It references CM in all cases. 1503=4XXX Randomly select processors for multiprocessors priority	CRD PPX is doing only CRD instructions. RW-D PPX is doing a mixture of CWD and CRD instructions. CWM PPX is doing only CWM instructions with a block length of 64. CRM PPX is doing only CRM instructions with a block length of 64. RW-M PPX is doing a mixture of CWM and CRM instructions. MIX PPX is doing a mixture of CWD, CRD, CWM, CRM, and EXN. XXXX - One of the following: RUN Processor is currently running a segment of the test. DONE Processor is done running a segment of the test. HUNG This PP is not done, but at least one of the other PPs is done. The QP idle program is no longer functioning; a deadstart is required to recover.

Mnemonic	Loading Mode	Parameters	Errors
MAP (Cont'd)		Address 1503=XXXX Do selected processors (same bit scheme as in 1502) 1504=Select processors which will reference CM (PP20-PP30) =1777 All processors selected to reference CM =XXXX Same bit scheme as in 1502 for PP20-PP30. 1505=Processors selected for multiprocessor priority (PPs 20 through 30) =XXXX Do selected processors (same bit scheme as 1504)	ECSS Error code (X1-CRM error) - (X2-CRD error) - (X4-CWM error) - (1X-CWD error). YYYY - Time to run a particular test segment. This is displayed only if (1500) = XXX1. Timing Error Displayed if address 1500 = XXX1. The processor(s) doing the priority read/write does not meet the timing criterion given under Description. Hung or ECS Refer to the preceding description of this error. ECS write abort Half exit occurred on the ECS write instruction (abort). ECS read abort Half exit occurred on an ECS read instruction (abort). ECS data error Address 4002_8, (CM) = actual data read and address 4003_8, (CM) = expected data.

Mnemonic	Loading Mode	Parameters		Errors
MAP (Cont'd)		Address 1506=0000	Check ECS data	
		=XXXX	Nonzero. Do not check ECS data	
		1510=XXX1	Section 0. No central program, single priority for CWD, CWM/CRM	
		=XXX2	Section 1. No central program, single priority for CWM, CRM, CWM/CRM	
		=XXX4	Section 2. No central program, multiprocessor priority	
		=XX1X	Section 3. CPU program active, same as section 0	

Mnemonic	Loading Mode	Parameters	Errors
MAP (Cont'd)		=XX2X Section 4. CPU program active, same as section 1 =XX4X Section 5. CPU program active, same as section 2 =X1XX Section 6. ECS transfers, similar PP activity to above sections	
PCM	Deadstart Binary, DSCL Binary Deck, ENS, Stand-Alone	Standard parameters	Display Running PPX 0P1 = XXXXXX 0P2 = XXXXXX INST = XX RS1 = XXXXXX (Appears on right screen.) RS2 = XXXXXX 0P1 and 0P2 — Two operands used (received) RS1 and RS2 — Resultants (RS1 - expected and RS2 - received)

Mnemonic	Loading Mode	Parameters	Errors
PCM (Cont'd)			INST = Octal code for the failing instruction. The beginning address of the simulation of the failing instruction is stored in address 1010_8, error count is stored in address 1007_8, and pass count is stored in address 1006_8. The first critical instructions (SHN, ADN, LMC) appear on left screen after being checked.
PCX	Deadstart Binary, DSCL Binary Deck, ENS, Stand-Alone	Address 1500=XXX1 Repeat subconditions =XXX2 Stop on error =XX1X Stop at end of test 1501=1XXX Repeat test =4XXX Repeat conditions 1506=Pass count 1507=Error count 1510=Address of failing instruction loop	Display Running PPX 0P1 = XXXXXX 0P2 = XXXXXX INST = XX RS1 = XXXXXX (Appears on right screen.) RS2 = XXXXXX

Mnemonic	Loading Mode	Parameters	Errors
PCX (Cont'd)			Display (Cont'd) 0P1 and 0P2 — Two operands used RS1 and RS2 — Resultants (RS1 expected and RS2 received) INST — Octal code for the failing instruction. The beginning address of simulation of the failing instruction is stored in address 1510, error count is stored in address 1507, and pass count is stored in address 1506. The first critical instructions (SHN, ADN, LMC) are checked and appear on the left screen after they are checked.

Mnemonic	Loading Mode	Parameters	Errors
PC1	Deadstart Binary, DSCL Binary Deck, ENS, Stand-Alone.	From absolute binary cards, deadstart from card reader 7760_8 words starting at address 0000. The deck must have exactly 51_{10} cards since the program checks for A=0 and channel empty. All available PPUs may be started by a space. One PPU at a time may be started by (PP1=A, PP2=B, PP5=E, etc.).	If error occurs, the program stops on a 0300. The CE must consult the listing to identify which instruction failed.
PC2	Absolute Binary, COMPASS Binary, ENS, LDR. PC2 is a stand-alone test. Channel parity switches must be on for all	Tag Name — Description I. P1 Control flags: =XXX2 CM instruction test option =XX1X Repeat test =XX2X Stop on error =X1XX Stop at beginning and end of test =1XXX Stop on memory parity error =4XXX Reload PPUs I. PP5E PPU enable bits (PPUs 0 - 11B)	Errors are isolated through the failing loop method (refer to publication no. 60409500).

Mnemonic	Loading Mode	Parameters	Errors
PC2 (Cont'd)	channels. CHX must have executed properly before attempting PC2.	Tag Name — Description I. PP6E — PPU enable bits (PPUs 20B - 31B) Keyboard Commands CE — Clear all error bits in the SCR Clear/set bits in parameter word I. P1 CES/SES — Stop on error CTS/STS — Stop at beginning and end of test CPS/SPS — Stop on PPU memory parity error CRT/SRT — Repeat test CRL/SRL — Reload PPUs	

Mnemonic	Loading Mode	Parameters		Errors
PC2 (Cont'd)			CCM/SCM CM instruction test option	
		DIX, YYYY	Change address of monitor PPU memory block X to YYYY.	
		RUX, YYYY	Change PPU X starting address to YYYY.	
		SPP, XX	Set and clear a PPU bit in parameter words	
		CPP, XX	I. PP5E and I. PP6E.	
		SPP/CPP	Set or clear all PPU bits in words I. PP5E and I. PP6E.	
		EPO, XXXX, YYYY	Enter data XXXX into master PPU memory at address YYYY.	
		RST	Restart the test.	
		RT	Return control to BETA SMM.	
		space	Start the test.	
		cr	Stop the test.	
		left blank key	Clear current keyboard entry.	

Mnemonic	Loading Mode	Parameters	Errors
PC2 (Cont'd)		+ Roll memory display forward. - Roll memory display backward.	
PPM	Deadstart Binary, DSCL Binary Deck, ENS, Stand-Alone.	Address 1000=0000 Stop and display errors after (50B) errors and display any errors found at the end of each test. =XXX1 Errors are displayed cumulatively up to the limit of the table (50B), but no stop is made. Table is reset to zero and restarted. =XXX2 Error stop is made after each error	Display Errors are displayed in the following format. Address Ex Pat Act Pat XXXX YYYY ZZZZ (XXXX)=Failing address (YYYY)=Expected pattern (ZZZZ)=Actual pattern Alarm Display = I/O idler failed XXXX (XXXX)=Failing address The test cannot be continued from this point.

Mnemonic	Loading Mode	Parameters		Errors
PMM (Cont'd)			Also displays any previous errors for that processor.	
		=XXX4	Stop after a section has been completed in a processor.	
		= XX1X	Stop at end of test.	
		=XX2X	Select PPS 2X speed (CYBER 170 only).	
		=XX4X	Enable error stop on PPU memory parity error or any other SCR fault condition.	
		1001=1XXX	Repeat test in all processors selected at beginning of test.	

Mnemonic	Loading Mode	Parameters		Errors
PMM (Cont'd)		Address 1001=2XXX	Enable a particular test section to be repeated in a processor.	
		1003= 1777	Processor flags for processing 0 through 10, bit 0 = processor 0, bit 1=processor 1,..., bit 9=processor 11B.	
		1004=1777	Processor flags for processors 20 through 31. Same bit assignment as for address 1003.	
		1010=0006	Section flags, bit 1=S register test and bit 2= worst pattern test.	

Mnemonic	Loading Mode	Parameters	Errors
PMX	LDR, Auto	None	If an error occurs, the test stops and must be restarted by an entry of N.60 (N=PP number the test resides in). Format Error EXXXX RYYYY XXXX = Expected data YYYY = Received data
PM1	Deadstart, Binary, DSCL Binary Deck, ENS, Stand-Alone.	None	Displays Example: LOC EMP REC PP LOG EXP REC PP xxxx xxxx xxxx PPxx xxxx xxxx xxxx PPxx 1356 7777 7677 PP01 1457 0000 0100 PP01 LOC = Location PP = PP number EXP = Expected REC = Received Test pattern has clobbered I/O alternator in processor XX, XX equals the PP containing the failing I/O idler. Test will resume after stop upon the depression of the spacebar.

Mnemonic	Loading Mode	Parameters		Errors
SSP	Deadstart Binary, DSCL, Binary Deck, ENS, Stand-Alone.	Address 1000=XXXX	Available PPUs (PPU0-11B). Bit 11=PPU0, bit 10=PPU1. etc. Set by the test.	Special SSP Display Entries C — Clears error stop parameter to allow program to continue. S — Sets stop on error parameter. Successive pressing brings up and suppresses the display of current central memory addresses in use and the contents of the A1 through A5 registers. Display is suppressed to speed the running of the test. + — Increments CM display addresses to cover XXXXX0-XXXXX7 for each PPU. / — Overrides internal CM display protection for the * entry. (CR) — Returns to the PS display to change parameters, etc. (space) — Return to the SSP display.
		1001=XXXX	Available PPUs (PPU20B-31B). Bit 11=PPU20B, bit 10= PPU21B, etc. Set by the test.	
		1002=XXXX	Section selection. Bit 1=section 1, etc.	
		1003=XXXX	PPU central memory usage area bias.	

Mnemonic	Loading Mode	Parameters	Errors
SSP (Cont'd)		Address 1004=XXX2 Stop on error. =XXX0 Continue after error. 1005=CPU bit selection: =XXX0 No CPU exchanges =XXX1 Exchange CPU-0 =XXX2 Exchange CPU-1 =XXX3 Exchange CPU-0 and CPU-1 1006=Upper 12 bits of central memory address limit: =1000 32K =1400 49K =2000 65K =3000 98K =4000 131K 1007=Loop count each section.	

Mnemonic	Loading Mode	Parameters	Errors
SSP (Cont'd)		Address 1010=Scope mode/repeat section flag. Bits 1 through 4 select sections 1 to 4 and bit 11 selects scope mode. 1011=Internal loop count. 1012=PPUs to read in section 4 PPS0. 1013=PPUs to read in section 4 PPS1. 1014=PPUs to write in section 4 PPS0. 1015=PPUs to write in section 4 PPS1. 1016=PPUs to exchange in section 4 PPS0. 1017=PPUs to exchange in section 4 PPS1. 1020=Single/block mode; =0000 Single word read/write instructions used in section 4.	

Mnemonic	Loading Mode	Parameters		Errors
SSP (Cont'd)		Address 1020 =0001	Block read/ write instruc- tions used in section 4.	
		1021≠0000	On SECDED error, read the chip select from the SCR and display.	

ECS TESTS

Mnemonic	Loading Mode	Parameters	Errors
DDP	LDR, Auto	Address 1500=XXX1 Repeat subcondition =XXX2 Stop on error =XXX4 Stop at end of section =XXX5 Stop at end of test 1501=1XXX Repeat test =2XXX Repeat section =4XXX Repeat condition =XXX1 Omit running display =XXX2 Speed up option =XXX4 Send errors to SMM dayfile 1502=CCEE Channel and equipment number 1504=Nonzero if there is another equipment on the same channel as one of the DDP ports being tested	Codes 1. Active XXXX — The channel is active when it should not be. XXXX is the last function sent to the DDP. 2. Inactive XXXX — The channel is inactive when it should not be. XXXX is the last function sent to the DDP. 3. Full XXXX — The channel is full when it should not be. XXXX is the last function sent to the DDP. 4. Empty XXXX — The channel is empty when it should not be. XXXX is the last function sent to the DDP. 5. Status AXXXX EYYYY ZZZZ — A = actual status, E = expected status, and Z = last function sent to the DDP before the status function.

Mnemonic	Loading Mode	Parameters	Errors	
DDP (Cont'd)		Address 1507=Section flags (sections 15 through 30), bit 0 = section 15, bit 1 = section 16, etc.† 1510=Section flags (sections 1 through 14), bit 0 = section 1, bit 1 = section 2, etc. 1512=Upper bits of first ECS address used for transfers 1513=Lower bits of first ECS address used for transfer (lower 3 bits = 0) 1514=Upper bits of last ECS address used for transfer 1515=Lower bits of last ECS address used for transfer 1516=CCEE, channel and equipment for first DDP port	6. Data AWWWW EXXXX YXXXX	W = word received, X = word expected, Y = position of 12-bit word in the 60-bit word, and Z = ECS address of transfer.
			7. AWWEXX R YYYYYY WZZZZZZZZ	Status from the DPP is incorrect after a flag register operation. WW = lower six bits of actual status, XX = lower six bits of the expected status, R = flag register number, and YYYYYY = contents of the flag register before the last flag word was sent in section 11; in section 4, this is what the contents of the flag register should have been before the last flag word was sent. ZZZZZZZZ = the last flag word sent.

†Section 20 should be run in uniport mode only.

Mnemonic	Loading Mode	Parameters	Errors	
DDP (Cont'd)		Address 1517=CCEE channel and 1520 equipment numbers for 1521 the second, third, and fourth DDP ports (The absence of a port is flagged with an entry of 7777.)† 1523=Upper bits of absolute last address in ECS 1524=Lower bits of absolute last address in ECS 7700=Flaw table. Enter the addresses of up to 31 known flaws, starting at 7700. The table is terminated by an address with bit 2^{23} set. The lower three bits of these addresses must be 0.	10. Error See I Display	Error has been detected by the CPU. Refer to I display for error code.
			11. INOUT IXXXX FYYYY ZZZZ	Channel disconnected during a block output. XXXX = the initial word count, YYYY = the final word count, and ZZZZ = the last function sent to the DDP.
			12. ININ IXXXX FYYYY ZZZZ	Channel is disconnected during a block input. XXXX = initial word count, YYYY = final word count, and ZZZZ = last function sent to the DDP.
			(C1) FLAG AXXXXXX EYYYYYY ZZZZZZZZ	(Flag register) Does not agree with the expected value sent from the PPU. XXXXXX = actual contents of the flag register, YYYYYY = expected contents of the flag register, and ZZZZZZZZ = last flag word sent from the PPU through the DDP.

†Section 20 should be run in uniport mode only.

Mnemonic	Loading Mode	Parameters	Errors	
DDP (Cont'd)			(C2) DATA AWWWW EXXXX BY WZZZZZZZZ	Data error: WWWW = 12-bit byte of actual data, XXXX = 12-bit byte of expected data, Y = position of 12-bit byte in a 60-bit word, and ZZZZZZZZ = ECS address.
			(C3) EXIT ON ECS WRITE WC XXXX A YYYYYYYY	Write abort from ECS. XXXX = initial word count and YYYYYYYY = ECS address.
			(C4) EXIT ON ECS READ WC XXXX A YYYYYYYY	Read abort or parity error from ECS controller. XXXX = initial word count and YYYYYYYY = ECS address.

Mnemonic	Loading Mode	Parameters			Errors
ECM	LDR, Auto	Use E display parameter area.			Messages
		Location	Default	Description	READ ABORT SECT X — Read abort detected in section X
		2 (DATA)	20	Data check pass count (that is, checksum every n passes)	HS READ ABORT X — Read abort in high speed read loop in section X
		3 (CKSUM)	20	Checksum pass (that is, checksum every n passes)	WRITE ABT SECT X — Write abort was detected in section X
		4 (SIZE)	10000	Buffer size	CHKSUM ERROR SECT X — Checksum error detected in section X
		5 (REP)	3	High speed read repeat count	DATA ERROR SECT X — Data error in section X; no read abort is detected
		6 (NWA)	0	Ignore write abort, restart if (6) = 0, and continue if (6) ≠ 0	ADDR aaaaaaaa (ECS address of the error)
		7 (SECT)	0	Repeat section	WROTE wwwwwwwwwwwwwwwwwwww (ECS word)
		10 (WS)	0	Write only (repeats write in current section)	READ rrrrrrrrrrrrrrrrrrr (ECS data read)
					DIFF ddddddddddddddddddddd (exclusive OR of r and w)
					P S YL XL XG B BK w
					P S Y XL X b bk w
					P = Plane, S = Side, XL = Drive line, XL = X drive line, XG = X group, B = Bay, BR = Bank, and W=word

Mnemonic	Loading Mode	Parameters			Errors
ECM (Cont'd)		Location	Default	Description	ECS II
		11 (RS)	0	Read only (repeats write in current section)	DATA ERROR SECT X — Same as previous error but display of bay, bank/word, and upper and lower logic card locations are given.
		12 (-)	1	Stop on error	ADDR aaaaaaaaaa WRITE wwwwwwwwwwwwwwwwwwww READ rrrrrrrrrrrrrrrrrrr DIFF ddddddddddddddddddddd U30 L30 B BK w All definitions remain the same except: U30 = Logic card location of upper 30 bits of failing address L30 = Logic card location of lower 30 bits of failing address
		13 (LOOP)	0	Loop on condition	
		14 (RETN)	0	Retain the last random number	
		15 (RAN)	220703125	Initial random number	
		16 (ECFL)		ECS field length (automatically determined in chassis 0)	
		17 (ECRA)	0	ECS RA	CM Error Table
		20 (CHASY)	0	Number of ECS chassis (automatically determined if not set)	Location 47 (SECNAM) Section letter Location 50 (ADDR) ECS failing address

Mnemonic	Loading Mode	Parameters			Errors
ECM (Cont'd)		Location	Default	Description	Location 51 (EXP) Data written
		21 (ERRORS)	10000	Number of data errors reported per buffer	Location 52 (ACT) Data read
		22 (SECT)	177777	Selected sections	Location 53 (DIF) XOR of data written and data read
		23 (ECS II)		Identify which banks are ECS II (that is, bit 0 = bank 0 is ECS II etc.)	Location 67 (ADW) CM address of data written
		24 (ECSCK)		Not equal to zero to run ECS II sections and addressing	Location 70 (ADR) CM address of data read
		25 (BANKS)		Number of ECS II banks available (no keyboard response required)	Location 71 (ERR) Number of data errors in current buffer
		26 (ONCPU)		≠0 if one of dual CPU to use all ECS	
		27 (DDP)		≠0 if DDP to run concurrently	

Mnemonic	Loading Mode	Parameters	Errors
ECS	LDR, Stand-Alone	Central Memory Parameters Address 3 = CCOE, channel and equipment number of line printer 4 = Ignore read abort/ parity errors if not equal to zero 5, 6, 7 = Diode stress parameters	Messages SET (12) = NO. OF ECS BKS ECS bits which are out of range for the system did not cause a write abort. RA-ECS REGISTER ERROR (16) = actual value (17) = expected value FL-ECS REGISTER ERROR BIT 17 NOT SET IN P BIT 17 DID NOT CLEAR IN P NO EXIT ON ILLEGAL INSTRUCTIONS CONTENT ERROR-EXPX AT 20 EXIT TO RA-EXPK AT 20

Mnemonic	Loading Mode	Parameters	Errors
ECS (Cont'd)		Address 10 = 20777377777B initially, each bit is used to select a test section (bit 0 = section 0, bit 1 = section 1, bit 2 = section 2, etc.) 11 = 400 ---0, test all banks of ECS = 0 through -XXXXXX, lower 16 bits each represent a particular bank; bit 0 represents bank 0, bit 1 represents bank 1, etc. 12 = 0 through 0XX, number of ECS banks in system; determined by the program if this number is zero 13 = 0, check all data in sections 10 through 26	PARITY ERROR NO EXIT TO RA-EXPK AT 20 DATA ERRORS NO WRITE ABORT NO READ ABORT ECS ACTIVITY-EXPK AT 20 WRITE ABORT-EXPK AT 20 ECS P REGISTER ERROR-DATA AT INBUF DATA ERROR READING ECS OUT OF RANGE TO INBUF READ ABORT WORD COUNT ERROR ON READING ZEROS WRITE ABORT READING ECS LOCKED OUT PP WRITE PP WRITE LOCKED OUT READING ECS READ ECS COMPLETED BEFORE EXCHAGE NO RESTART AFTER FIRST EXCHANGE ECS RA NOT ADDED TO X0 WORD COUNT ERROR-ADD 777 TO (B7) EXCHANGE ADDRESS ERROR-DATA AT INBUF PP R/W ERR-DATA AT INBUF ABORT ON CLEAR GLOBAL REGISTER DATA TRANSFER ON X0 FUNC

Mnemonic	Loading Mode	Parameters	Errors
ECS (Cont'd)		Address 13 = Not equal to zero, do not check data in sections 10 through 26 (Cont'd)	ABORT ON SET GLOBAL REG ABORT ON STATUS GLOBAL REG ACCEPT ON STATUS GLOBAL ABORT ON R/S GLOBAL REG
		14 = Not equal to zero, do only writes and no reads	ACCEPT ON R/S GLOBAL REG LP NOT READY ECS TO CM ERR-CHECK INBUF,X0,A0
		= Equal to zero, do writes and reads of data	CM TO ECS ERR-CHECK INBUF,X0,A0 CHECK INBUF-EXP 2X(B7) WDS OF ADDR PE WENT AWAY-X0, B7 SET FROM LAST PE IN BLOCK
		15 = Not equal to zero, do only reads and no writes	WRITE ABORT-CPU1 013 EXECUTION CAUSED GLOBAL REGISTER SET
		= Equal to zero, do reads and writes of data	FLAG ERR ON 013 FOLLOWED BY GR CLEAR FNC
		40 = XXXXXX, global register flag bits to be used by this computer	FLAG ERR ON 013 FOLLOWED BY GR SET FNC FLAG ERR ON 013 FOLLOWED BY GR STATUS FNC
		44-47 = Operator's pattern for section 17	FLAG ERR ON 013 FOLLOWED BY GR RDY/SEL FNC
		44 = Pattern word for ECS word 1, CM words 1, 2, 3, 4	ABORT ON ECS WRITE FOLLOWING 013 ABORT ON ECS READ FOLLOWING 013 013 FAILED TO EXECUTE

Mnemonic	Loading Mode	Parameters	Errors
ECS (Cont'd)		Address 45 = Pattern word for ECS word 1, CM words 5, 6, 7, 8 46 = Pattern word for ECS word 2, CM words 1, 2, 3, 4 47 = Pattern word for ECS word 2, CM words 5, 6, 7, 8 50-57 = MASR for data checking in sections 10 through 26, initially all 77-77 74 = Parameter for section 24 (random) 75 = Number of times to loop in section 24 100-277 = Flaw table, initially set to zero	GR SET FNC EXECUTION ERROR GR READY/SELECT FNC EXECUTION ERROR PPX CHANNEL CLOBBERED PPX HAD DATA ERRORS ON READ/WRITE CP0 READ TOO MANY WORDS FROM ECS CP1 READ TOO MANY WORDS FROM ECS PARITY ERROR EXPECTED-DID NOT OCCUR PARITY ERROR OCCURRED-NOT EXPECTED **NOTE** Due to the number of possible errors, refer to publication no. 60160600 for detailed descriptions of the individual errors.

MAGNETIC TAPE TESTS

Mnemonic	Loading Mode	Parameters	Errors
ATC	Stand-Alone, LDR, Auto Section 23 cannot run on any machine that does not have parity.	MCP CON 0012B MCP1 CON 1000B MCP2 CON 0700B MCP3 CON 77B MCP4 DATA 0 MCP5 DATA 0 MCP6 DATA 0 MCP7 DATA 603B MCP10 DATA 7777B MCP11 DATA 0 Address 1500=XX2X End subsection stop =XX1X End test stop =XXX4 End section stop =XXX2 Error stop 1501=XXX1 Do not display run message =XXX2 Utility mode =XXX4 Speed up option =XX1X Errors to print =1XXX Repeat test =2XXX Repeat section =4XXX Repeat condition	Message Format AABB, SYYSSZZ, PCCCC, LFNDDDD, UEE AA Classification of error BB Specifier to the failing function YY Section number ZZ Subsection number CCCC Program address from which error originated DDDD Code of function last attempted (excluding status) EE Unit last selected by the test Usage Dictionary The following messages are in six classifications: read (RD), write (WT), general functions (GF), channel (CH), test information (TI), special purpose (SP), and data errors (DE). Each error code consists of an alpha classification and a numeric specifier. These message codes point to the error in the function being performed when the error occurred.

Mnemonic	Loading Mode	Parameters		Errors	
ATC (Cont'd)		Address 1502=CCEE	Channel/ equipment	Error Code	Message and Description
		1503=0XXX	Units to test (bit 0=unit 0)	RD00	COPY CODE TRANSLATION READ MEMORY
		1504=0XXX	Units to test (bit 0=unit 10)	RD01	COPY CODE TRANSLATION WRITE MEMORY
		1505=4XXX	Do not display history table	RD02	DETAILED STATUS
				RD03	UNIT STATUS
		=2XXX	Stop at beginning/end utility	WT00	LOAD CODE TRANSLATION READ MEMORY
		=1XXX	Utility step	WT01	LOAD CODE TRANSLATION WRITE MEMORY
		1507=XXXX	Sections 30 through 15	WT02	SHORT WRITE
		1510=XXXX	Sections 14 through 01	WT03	WRITE TAPE MARK
				WT04	WRITE
		1511=XXXX	Sections 44 through 31	GF00	CLEAR UNIT
				GF01	CONNECT
		Controller maintenance panel switch positions:		GF02	FORMAT UNIT
				GF03	HIGH READ CLIP
				GF04	HYPER READ CLIP
		Switch	Position	GF05	LOW READ CLIP
				GF06	LOOP WRITE THROUGH DCU
		ON-LINE/OFF-LINE	ON-LINE	GF07	LOOP WRITE THROUGH UNIT
				GF10	MCGO

Mnemonic	Loading Mode	Parameters		Errors	
ATC (Cont'd)		Switch	Position	Error Code	Message and Description
		FORCE CH. P.E./ OFF	OFF	GF11	NORMAL READ CLIP
		ERROR STOP/OFF	OFF	GF12	OPPOSITE PARITY
		CONT/SINGLE STEP	CONT	GF13	OPPOSITE DENSITY
		SWEEP/N/LOAD	N	GF14	RELEASE UNIT
		TEST MODE/OFF	OFF	GF15	FORCE DATA ERROR
		STOP/SYNC	SYNC	GF16	SET EVEN CHANNEL PARITY
		SINGLE STEP/ CONTINUE	CONTINUE	GF17	SET EVEN READ PATH PARITY
				GF20	SET TRANSFER CHECK CHARACTERS
				GF21	STOP MOTION
				GF22	TEST VELOCITY
				CH0X	The channel was expected to be/go active. X=0 General X=1 Not used X=2 Block I/O instruction exit without nonzero
				CH1X	The channel was expected to be/go inactive. X=0 General X=1 Not used

Mnemonic	Loading Mode	Parameters	Errors
ATC (Cont'd)			Error Code — Message and Description X=2 No response to status function CH2X — The channel was expected to be/go full. X=0 General CH3X — The channel was expected to be/go empty. X=0 General TI15 — No units have been selected for test. TI23 — The history code table has overflowed. TI25 — A block transfer instruction has exited with the A register nonzero. TI31 — Refer to TI25. TI32 — The status adjust code for the present function exceeds the range of the table. TI40 — The unit selected is either busy or not ready.

Mnemonic	Loading Mode	Parameters	Errors
ATC (Cont'd)			Error Code — Message and Description DE00 — The data read from the code conversion read memory was incorrect. DE01 — The data read from the code conversion write memory was incorrect. DE02 — DETAILED STATUS DE03 — UNIT STATUS SP01 — Channel pause after 320 words was longer than expected. SP02 — Channel pause was less than expected.
MMT	Stand-Alone, LDR, Auto	Address 1500=XXX1 Repeat function =XXX2 Stop on error =XXX4 Stop at end of section =XX1X Stop at end of test =XX2X Stop at beginning of section	All error messages are of the following format MMT XXYY Ua Cbb XX = Section number YY = Subsection letter a = Unit number bb = Condition code numeric, last function code issued

Mnemonic	Loading Mode	Parameters		Errors
MMT (Cont'd)		Address 1500=X1XX	Suppress channel drop on error	If bb is numeric, it is the last function code issued; otherwise, bb=Wx after a write operation and bb=Rx after a read. The mode of the read or write is indicated by x. x = 0 Forward 1 Reverse 2 Memory 4 Conversion 8 Nonstop MMT NO TAPE AVL NLP (No load point) NNEC - NRZI error correction failure NO COLD START NO DATA XFER NO INCL NO INT OVERRIDE NO NONSTOP FM EOT NOT CLEARED L DAT N BSY NPEC RDY AFTER REW UNL
		=X2XX	Suppress channel drop while unit is busy	
		=X4XX	Suppress data check after the first data error is detected	
		1501=XX40	Run all 657 densities (800 only if void)	
		=X1XX	Run NRZI only on 659's	
		=X2XX	Run phase only on 659's	
		=X4XX	Parity-enhanced 6681-F or DCC (CYBER 170)	
		=1XXX	Repeat test	
		=2XXX	Repeat subsection	

Mnemonic	Loading Mode	Parameters		Errors
MMT (Cont'd)		Address 1502=CCEE	Use channel (CC = controller and EE = equipment)	RJT FC XXXX (XXXX=function code) STATUS - Status error in utility TPE - Transmission parity WXXX RYYY WD ZZZZ
		1503=XXXX	If zero, run on all ready units, or bit 0 = unit 0, bit 1 = unit 1, etc.	GND TK8, NE GEC MMT RELEASE 9 BIT SW NEGATE ERR. COR. TURN OFF CAPSTAN ON UNIT X DEN REP/REJ ERR XT XS
		1506=XXXX	6681 select code	CH ER X FYYY BSY
		1507=XXXX	Select sections 12 through 23 (bit 0 = section 12, bit 1 = section 13, etc.)	N RDY NO BUSY RJT NO CON RJT NO ERR NO INT
		1510=XXXX	Select sections 0 through 11 (bit 0 = section 0, bit 1 = section 1, etc.)	NO LOST DATA EOT FPND S2XXXX E3401 MPE NO UNITS RDY

Mnemonic	Loading Mode	Parameters		Errors
MMT (Cont'd)		Address 1511=XXXX	Select sections 24, 25, and 26 (bit 0 = section 24, bit 1 = section 25, etc.)	RD TM DATA ER READY ERR SW AXXXX EYYYY (XXXX=actual status, YYYY=expected) TOO MUCH DATA UNX INT
		1525=XXXX	FCOs installed	ERR.COR. ENABLE
		=XXX1	CA26148 BCD	GROUND BIT X
		=XXX2	CA26681 FM with reverse read set	MMT SET 9 BIT SW SET NORMAL
		=XXX4	CA26846 reverse read error correction	TURN ON CAPSTAN ON UNIT X
		=XX1X	CA29235 unit release 2 by 8	**NOTE** Due to the number of possible errors, refer to publication no. 60160600 for detailed information of the preceding errors.
		=XX2X	CA30580 programmable clipping level	
		=XX4X	CA32119 preample/postample error	
		=X1XX	CA34279 cold-start	

Mnemonic	Loading Mode	Parameters		Errors
MMT (Cont'd)		Address 1525=2XXX (Cont'd)	Nonread alternate FMs and records in phase	
		=4XXX	Interrupt override	
MTA/MTB	Stand-Alone, Auto. Upon typing MTA, a message that no idle PPU can be found into which MTB can be loaded or the message HIT SPACE BAR TO CONTINUE will appear.	Address 1500=XXX2	Stop on error	Error messages always appear at the bottom of the screen, following large running display. If the running display is suppressed to speed the running of the test, the error messages appear in the same place. All error messages are of the following format. ERROR=aabb ScccSSdd Uee LFNffff Pgggg Dhhhh aa = RD Read error WT Write error DE Data error FE Function error CH Channel error CF Connect error FF Format function error TM Tape motion error
		=XXX4	Stop at end of section	
		=XX1X	Stop at end of test	
		=XX2X	Stop at end of subsection	
		=4XXX	Abort current section; go to next selected section	
		1501=XXX1	Unload tapes at end of test	
		=XXX2	Enable utility mode	
		=XXX4	Speedup option	

Mnemonic	Loading Mode	Parameters	Errors
MTA/MTB (Cont'd)	When the space bar is pressed, the normal parameter display will appear. After the space bar is pressed again, the test begins. The following are requirements of the test. 1. The ON-LINE/OFF-LINE switch must be in the ON-LINE position.	Address 1501=XX1X Dump errors on printer =XX4X Repeat subsection =1XXX Repeat test =2XXX Repeat section =4XXX Repeat condition 1502=CCEE Channel and equipment numbers 1503=0XX1 Select tape unit 0 =0XX2 Select tape unit 1 ⋮ ⋮ ⋮ ⋮ =02XX Select tape unit 7 1504=XXX1 Select tape unit 10	bb = Identifies function being performed. cc = Current section dd = Current subsection ee = Unit number ffff = Last hardware function sent gggg = Program address hhhh = Current density (556, 800, 1600, or 6250)

Mnemonic	Loading Mode	Parameters	Errors
MTA/MTB (Cont'd)	2. The ERROR STOP switch must be in the OFF position. 3. The tape unit access switches must be enabled for those units to be tested. 4. All tape units to be tested should be ready with a write ring in the tape reel.	Address 1504=XXX2 Select tape unit 11 ⋮ ⋮ ⋮ ⋮ =X4XX Select tape unit 17 1505=XXX1 Eliminate display =XXX2 Stop on first data error only =XX1X Run GCR and NRZI =XX2X Run 800 and phase =1XXX Place utility or repeat condition mode into step mode =2XXX Stop at beginning of utility/history table 1506=Not used	

Mnemonic	Loading Mode	Parameters	Errors
MTA/MTB (Cont'd)		Address 1507=XXX1 Select section 15 =XXX2 Select section 16 . . . . =4XXX Select section 30 1510=XXX1 Select section 1 =XXX2 Select section 2 . . . . =4XXX Select section 14 1511=XXX1 Select section 31 =XXX2 Select section 32 . . . . =4XXX Select section 44	

Mnemonic	Loading Mode	Parameters	Errors
MTT	Deadstart Binary, DSCL Binary Deck, ENS, Stand-Alone, Auto	Address 1500, 1501, 1502=Standard SMM parameters except that 1500=XX2X - Mode I connect and function. 1503=0000 Run all available units =0XXX Run units 0X/ bit selection 1504=0XXX Run units 1X/ bit selection 1505=Unused or MAC select code 1506=6681/6684 select code 1507=4XXX Run test in fast mode 1510=XXXX Section selection bits	Messages CCddEf, Uvv, Sppt STxxxx, Cyyyymmmm d = Channel number f = Equipment number v = Unit number p = Current section t = Current subsection (A through Z) x = Current equipment status y = Current 6681/DCC status m = Message Normal Message — Description BUSY — Normal running message FRXX — Function XX rejecting; normal unless constant CNRJ — Connect reject; normal unless constant NRDY — Unit not ready LOAD — Initial message to select TAPES — parameters

Mnemonic	Loading Mode	Parameters		Errors	
MTT (Cont'd)		Address 1511 = 4XXX	Recover (9 times) write parity error	Normal Message	Description
		= 2XXX	Controlled backspace option	END TEST	End of test
		= 1XXX	Do not check data on reads	END SEC	End of current section
		= X4XX	No running display rejects and functions are displayed	REQUEST MT	Tape unit request for on-line operation
		= X2XX	Reverse read capability	RQCH	Requesting tape channel from SMM
		= X1XX	Use 6684 test patterns	Error Message	Description
		= XX4X	Run patterns test	RLD	Lost data on read
		= XX2X	37.5 ips tape unit	RPE	Read parity error
		= XX1X	75 ips tape unit	NEOP	No end of operation status
		= XX0X	150 ips tape unit	FEOF	False file mark status
				TPEX	Transmission parity error X=C (connect), X=F (function), X=W (write), X=R (read), X=absent (wait condition)
				WLD	Lost data on write

Mnemonic	Loading Mode	Parameters	Errors
MTT (Cont'd)		Address 1511 (Contd) = XXX6 800 bpi = XXX3 556 bpi = XXX4 200 bpi = XXX0 Run all densities	Error Message — Description WPE — Write parity error (displayed if 1511 ≠ 4XXX) EOT — End of tape - section restarts NEOF — No file mark status PERF — Parity error on read file mark reverse in BCD mode BKSP — Load point or file mark status encountered after a backspace RFFE — Read file mark forward data error, should be 1700_8 RLE — Word count in a register not correct after read WLE — (A) not zero after write CRDI — Cannot clear ready not busy interrupt CEOI — Cannot clear end of op interrupt NABI — No abnormal end of op interrupt FEOP — EOP status is constant of is set immediately after initiation of an operation PSBS — Parity error status on skip bad spot function

Mnemonic	Loading Mode	Parameters	Errors
MTT (Cont'd)			Error Message — Description
			IE — Channel inactive, should have been active
			NOBZ — Busy status not up after initiation of operation
			NPBF — No parity err on write file mark in binary mode unrecoverable write parity error (9 tries max)
			UWPE — Displayed if (1511)=4XXX
			NRXX — Function XX did not reject when unit busy
			EOPT — End of operation status was timed out
			CLRE — Status not X000 after clear function
			RFRE — Read file mark in reverse data error, should be 17_8
			NRDI — No ready not busy interrupt
			NEOI — No end of operation interrupt
			CABI — Cannot clear abnormal EOP interrrupt
			NLDP — No load point status

Mnemonic	Loading Mode	Parameters	Errors
MTT (Cont'd)			Error Message — Description NRPE — No read parity error after reading a binary record in BCD mode or vice versa AE — Channel active, should have been inactive XXDN — Incorrect density status, XX= selected density PECF — Parity error on write file mark in BCD mode WPXX — Recovered write parity error on XX number of tries (9 max), displayed if 1511=4XXX NOLD — No lost data status BZTO — Not busy status was timed out RELE — Status not X000 after release function NPRF — No parity error on read file mark in binary mode DATA ERRORS FORMAT — Displayed if location 1511≠1XXX INF B=XXXX G=WWWW XXXX = Bad information received WWWW = Information written

Mnemonic	Loading Mode	Parameters	Errors
MTT (Cont'd)			Error Message — Description NO TAPES — Test cannot find a unit that is ready, unreserved, connectable, and write enable status. Current status in in location 0037. FE — Channel full before output FA — Channel full after 100 microseconds EI — Channel empty before input DCC ERR X PAT Y — X = A ACN did not activate channel; = B DCN did not deactivate channel; = E Channel was active after FAN; = F Channel hung full after status function was sent

Mnemonic	Loading Mode	Parameters	Errors	
MTT (Cont'd)			Error Message	Description
			X = G	Channel was empty after status function was sent
			= H	Normal parity, mode I parity error
			= I	Normal parity, mode II parity error
			= J	Zero parity, mode I parity error occurred but should not have occurred
			= K	Zero parity, mode II parity error occurred but should not have occurred.
			= L	Zero parity, mode I did not receive expected parity error
			= M	Zero parity, mode II did not receive expected parity error

Mnemonic	Loading Mode	Parameters	Errors
MTT (Cont'd)			Error Message: A NR EXXXX DYYYY Description: Y = 1 to 4 for pattern used when error occurred (1 - 1201B, 2 - 1300B, 3 - 1200B, and 4 - 1700B) A = C for connect, F for function, D for data X = Expected status Y = Actual DCC/6681 status

Mnemonic	Loading Mode	Parameters	Errors
RGG	Deadstart Binary, DSCL Binary Deck, ENS, Auto	Address 1502 = CCOE, channel and equipment 1503 = OOUN, unit (00 through 17) 1504 = OOOS, S is system ID (0 through 7) 1507 = SSNI, SS is section select bits (Bit 0) = Section 1, fixed delay, normal vacuum (Bit 1) = Section 2, same as section 1 with reduced vacuum (Bit 2) = Section 3, incremental delay, normal vacuum	Errors are of the following format. S 1 CH XX EQ YYYY DIR GAP RC SR LR SE DE DLY MIN MAX V F .32 250 075 000 010 000 004 016 024 N Line 1 Identifies the system, channel, and equipment being tested. Line 2 Header describing the data in line 3 and subsequent lines. (All values are in decimal values.) DIR F=forward, R=reverse GAP Gap size in 100th of inches RC Record count, number of records read SR Number of short records read LR Number of long records read SE Number of records that were of proper length, but had a status error, parity error, lost data, load point, or end of tape DE Number of records with correct length

Mnemonic	Loading Mode	Parameters	Errors
RGG (Cont'd)		Address 1507 = (Bit 3) = Section 4, same as section 3 with reduced vacuum (Bit 4) = Not used (Bit 5) = Run on a modified 659 unit N = Maximum number of gaps to be run in each direction I = Gap increment in 100th of inches 1510 = FG RG, FG = forward starting gap in decimal 100th of inches and RG = reverse starting gap in decimal 100th of inches	

Mnemonic	Loading Mode	Parameters	Errors
TCT	Stand-Alone, Auto	Address 1501 = Bit 0 - Bypass errors from current record when set = Bit 1 - Bypass current pattern errors = Bit 2 - Bypass unit errors 1505 = 000X, X is the system ID (0 through 7) 1506 = 2000B-6681 select code 1507 = Bit 11 - Initial write Bit 10 - Write Bit 9 - Read Bit 8 - Test reverse Bits 7, 6, 5 - Not used Bit 4 - Nine track Bit 3 - 1600 cpi Bit 2 - 800 bpi Bit 1 - 200 bpi (illegal on 659's) Bit 0 - 556 bpi (illegal on 659's)	Messages CHaa Ebbbb Dc RPE de Pfff Sg CHhh Eiiii READ PARITY ERROR aa = Channel of unit reading or writing bbbb = Connect code of unit reading or writing c = Density being tested (2, 5, 8, or 1) = (200, 556, 800, or 1600) d = Direction of read (F or R for forward or reverse) e = Pattern being read or written (A through F) fff = Current file number indicates the file currently being read g = System ID of the system that wrote the data read hh = Channel of the unit that wrote the data read iiii = Connect code of the unit that wrote the data *CHaa Ebbbb Dc WPE e WRITE PARITY ERROR *CHaa Ebbbb Dc-FUNCTION REJECTED *CHaa Ebbbb Dc-CONNECT REJECTED

Mnemonic	Loading Mode	Parameters	Errors
TCT (Cont'd)		Address 1510 = Bits 0 through 2 - Equipment for first channel Bits 3 through 7 - First channel Bits 8 through 11 - Select units 14 through 17 1511 = Bits 0 through 11 - Select units 0 through 13 1512 and 1513 Same as 1510 and 1511 except for second channel 1514 and 1515 Same as 1510 and 1511 except for third channel 1516 and 1517 Same as 1510 and 1511 except for fourth channel **NOTE** This test will also run under SCOPE. Refer to publication no. 60160600 for SCOPE parameters.	*CHaa Ebbbb Dc RDE de Pfff Sg CHhh Eiiii-READ DATA ERROR DATA EXP xxxx DATA RCVD xxxx BYTE xxxx *CHaa Ebbbb Dc-NO EOF STATUS AFTER WEOF *CHaa Ebbbb Dc PERRd e Pfff Sg CHhh Eiiii-POSITION ERROR *CHaa Ebbbb NO EOP e-END OF OPERATION STATUS DID NOT OCCUR

PRINTER TESTS

Mnemonic	Loading Mode	Parameters	Errors
FTP	Stand-Alone, Auto	Address 1500=XXX2 Stop on error =XXX4 Stop at end of section =XX1X Stop at end of test =XX2X Stop at beginning of section 1501=4XXX Repeat condition =2XXX Repeat section =1XXX Repeat test 1502=CCOE, channel and equipment if only one printer is to be run, and 1503=0000. If 1503 is not zero, the channel number (CC) is saved and the equipment (E) is ignored. 1503=000 0XX XXX XXX, X is the bit equivalent of the equipment number (bit 0 = equipment 0, bit 1 = equipment 1, etc.)	Messages LPcce Sss STxxxx CzzzzPpppp Rcomment c = Channel number e = Equipment number s = Current section x = Last copied equipment status or 7777 if a channel error z = Last copied converter status p = Program error location R = Repeat condition bit set (1501=4XXX) comment = May be any of the following. RESERVE CHAN ACT (Channel was active before first command was issued to the channel.) CHANNEL ACTIVE (Channel was found active when it should not have been.) CH ACT, CH FNffff (Channel remains active after channel function ffff.) INACT AFTER ACN (Channel found inactive after an activate channel.)

Mnemonic	Loading Mode	Parameters	Errors
FTP (Cont'd)		Address 1504=X1XX Lines/inch for section 5 (0=8 lines/inch, 1=6 lines/inch) =Bits 0 through 2 = train type. 0 or 1 = 596-1, 63 characters 2 = 956-2, 48 characters 3 = 956-3, 48 characters 4 = 956-4, 63 characters 5 = 596-5, 63 characters 6 = 596-6, 95 characters 1505=XXX1 Parity enhanced 6681 (6681-F/DCC) 1506= 2000, 6681 select code 1507= Bits 0 through 8, sections 14 through 24 1510=Bit 0=section 0, fill train image and bits 1 through 11=sections 1 through 13	CHANNEL INACTIVE (Channel inactive when it should have been.) FULL BEFORE OUT (Channel found full before an output was executed.) STILL FULL, OUT (Channel remains full after an output.) STILL EMPTY, IN (Channel remains empty after an input function was issued.) STILL FULL, INPUT (Channel remains full after an input.) ACTIVE AFTER DCN (Channel remains active after a deactivate command.) WAITING READY (Printer is not ready.) INT LINE, NO STAT (6681 status indicates interrupt, no equipment interrupt status.)

Mnemonic	Loading Mode	Parameters	Errors
FTP (Cont'd)		Address 1511= BCD code for first character in section 12 = full line of single character	STAT, NO INT LINE (Equipment status indicates interrupt; 6681 status shows no interrupt.) RNB DID NOT CLR (Section 3, ready not busy interrupt did not clear.) EOP DID NOT CLR (End of operation interrupt did not clear.) ABN DID NOT CLR (Abnormal end of operation interrupt did not clear.) STATUS EXP YYYY (Received status does not agree with received status YYYY.) EXT REJECT CON (A connect rejected.) EXT REJECT F=ff (Function ff rejected.) INT REJECT (An internal reject occurred.)

Mnemonic	Loading Mode	Parameters	Errors
FTP (Cont'd)			TRAN PARITY (A transmission parity error occurred.) NO EXT REJ F=ff (External reject did not occur for function ff.) NO INT REJ (Internal reject did not occur.) PRINT ERROR (A print error status is indicated.) ABORT TEST [Warning that test will not be continued. If repeat test (MCP1=1XXX) bit is not set, the test returns control to SMM. If set, the test restarts.]

Mnemonic	Loading Mode	Parameters	Errors
LP1	Stand-Alone, Auto	Address 1500=XXX2 Stop on error =XXX4 End of section stop =XX1X Stop at end of test 1501=4XXX Repeat condition =2XXX Repeat section =1XXX Repeat test 1502=CCOE, channel and equipment number 1503=000 0XX XXX XXX, X is bit equivalent of the equipment number, (if 1503≠0, only the channel is used from 1502) 1505=XXX1 Parity-enhanced 6681 (6681-F/DCC) 1506=6681 select code	Messages The following messages contain format: LPcce Sss STxxxx Ppppp cc = Channel of the 3555 e = Equipment number of the 3555 ss = Current section xxxx = Last copied equipment status or 7777 if a channel error pppp = Location in program where the error occurred RESERVE CHAN ACT CHANNEL ACTIVE CH ACT, CH FNffff (ffff=channel function) INACT AFTER ACN CHANNEL INACTIVE

Mnemonic	Loading Mode	Parameters	Errors
LP1 (Cont'd)		Address 1507=Bit 11=0, select six lines per inch. If bit 11=1, select eight lines per inch. =Bit 9, 10=0 or 1=63 characters, 2=48 characters, and 3 = 48HN character train =Bits 0 through 6 = select sections 14 through 23 1510=Bits 1 through 11=select sections 1 through 13 1511=BCD code for first character in section 12 (full line of single character), XXX1-fill image	FULL BEFORE OUT (Channel full before output executed.) STILL FULL, OUT (Channel remains full after an output.) STILL EMPTY, IN (Channel remains empty after an input function.) STILL FULL INPUT (Channel remains full after an input.) ACTIVE AFTER DCN (Channel remains active after a deactivate command.) WAITING READY (Stop on error is not selected and printer is not ready.) INT LINE, NO STAT (6681 status indicates interrupt but no equipment interrupt status.) STAT, NO INT LINE (Equipment status indicates interrupt but 6681 status shows no interrupt.) RNB DID NOT CLR (Ready not busy interrupt did not clear, section 3.) EOP DID NOT CLR (End of operation interrupt.) ABN DID NOT CLR (Abnormal end of operation interrupt.) STATUS EXP YYY (Expected status does not agree with status received.)

Mnemonic	Loading Mode	Parameters	Errors
LP1 (Cont'd)			nnn, ERR, Cccc Pppp (Print error occurred and nnn errors were found. The first error found was code ccc in position ppp.) EXT REJECT CON (A connect rejected.) EXT REJECT F=ff (Function ff rejected.) INT REJECT (An internal reject occurred.) TRAN PARITY (A transmission parity error occurred.) NO EXT REJ F=ff (An external reject did not occur for function ff.) NO INT REJ (An internal reject did not occur.) PR ERR, Eeee Rrrr (A print error which should have produced eee errors gave rrr errors.) NO IDENT TRAIN (Test could not identify train type; 63-character train is assumed.) NO FIND, PRINT ER (Print error is in status but input yielded no code error.) NO LEVEL 9 STAT (Section 2 showed that no level 9 status occurred.) NO COINCIDENT (Section 2 found no coincident status.)

Mnemonic	Loading Mode	Parameters	Errors
PFC	Stand-Alone, Auto	Address 1500=XXX2 Stop on error =XXX4 Stop at end of section =XX1X Stop at end of test =XX2X Stop at beginning of section 1501=4XXX Repeat condition =2XXX Repeat section =1XXX Repeat test 1502=CC0E Channel and equipment number if only one printer 1503=000 0XX XXX XXX, X is the equivalent of the equipment number (if 1503≠0, only the channel from 1502 is used) 1504=X1XX 6 lines per inch (section 5) =X0XX 8 lines per inch (section 5); N/A for PFC printer	Normal Messages TEST FTP (Stop at beginning of test for parameter entries.) BEG OF SEC XX [Stop at beginning of section nn if MCP, bit 4 (1500=XX2X) parameter is set.] END OF SECTION XX [Stop at end of section nn if MCP, bit 2 (1500=XXX4 is set.] END TEST [Stop at end of test if MCP, bit 3 (1500=XX1X) is set.] Error Messages Error messages are prefaced with a line that is formatted as follows: LPcce Sss STxxxx Ppppp Rcomment c = Channel number e = Equipment number s = Current section x = Last copied equipment-status or 7777 if a channel error p = Location in the program where error occurred R = Appears when repeat condition bit is set (1501=4XXX)

Mnemonic	Loading Mode	Parameters	Errors
PFC (Cont'd)		Address 1504=XXX0 596-1, 63-character train =XXX1 596-1, 63-character train =XXX2 596-2, 48-character train =XXX3 596-3, 48-character train =XXX4 596-4, 63-character train =XXX5 596-5, 63-character train =XXX6 596-6, 95-character train =XXX7 Not applicable 1505=2000 6681 select code 1507=Bits 0 through 7 set to select sections 14 through 23. Bit 8 set to select section 24 (not defaulted).	comment = May be one of the following messages. RESERVE CHAN ACT (The channel was found active before the first command to the channel. The test will not continue.)† CHANNEL ACTIVE (The channel was found active when it should not have been. The test will not continue.)† CH ACT, CH FNffff (The channel remains active after the channel function ffff. The test will not continue.)† INACT AFTER ACN (The channel was found inactive after an activate channel. The test will not continue.)† CHANNEL INACTIVE (The channel was inactive when it should not have been. The test will not continue.)† FULL BEFORE OUT (The channel was found full before an output was executed. The test will not continue.)†

†After message is issued (unconditional stop), the test issues the ABORT TEST message.

Mnemonic	Loading Mode	Parameters	Errors
PFC (Cont'd)		Address 1510=Bit 0 set selects section 0, fill train image is always selected. =Bits 1 and 3 through 11 select sections 1 and 3 through 11, and bit 2 selects section 2, which is not defaulted. 1511=BCD code for first character in section 12 (full line of single character) 1512=0000 Normal printer ≠0000 PFC printer	STILL FULL, OUT (The channel remains empty after an input function was issued. The test will not continue.)† STILL EMPTY, IN (The channel remains empty after an input function was issued. The test will not continue.)† STILL FULL, INPUT (The channel remains full after an input. The test will not continue.)† ACTIVE AFTER DCN (The channel remains active after a deactivate command. The test will not continue.)† WAITING READY (Stop on error is not selected, and the printer is not ready.) INT LINE, NO STAT (6681 status indicates an interrupt, but there is no equipment interrupt status.) STAT, NO INT LINE (Equipment status indicates an interrupt, but 6681 status shows no interrupt.) RNB DID NOT CLR (In section 3, a ready not busy interrupt did not clear.)

†After message is issued (unconditional stop), the test issues the ABORT TEST message.

Mnemonic	Loading Mode	Parameters	Errors
PFC (Cont'd)			EOP DID NOT CLR (End of operation interrupt did not clear.) ABN DID NOT CLR (Abnormal end of operation interrupt did not clear.) STATUS EXP yyyy (Status expected yyyy does not agree with status received.) EXT REJECT CON (A connect rejected.) EXT REJECT F=ff (Function ff rejected.) INT REJECT (An internal reject occurred.) TRAN PARITY (A transmission parity occurred.) NO EXT REJ F=ff (An external reject did not occur for function ff.) NO INT REJ (An internal reject did not occur.) PRINT ERROR (A print error status is indicated.) ABORT TEST [Test will not be continued. If a repeat test, section, or condition (MCP1=1XXX, 2XXX, 4XXX) bit is not set, the test returns control to SMM. If a bit is set, the test restarts.]

Mnemonic	Loading Mode	Parameters	Errors
PFC (Cont'd)			WRONG TRAIN NO., RESET LOC 1504 AND GO (If train number 7 is selected, this message is provided. Reset train number to 1 through 6 only and go.) VALID NOT CLEAR (Issuing a valid format function did not clear a nonvalid format function PFC status error.) COINCIDENT ERROR (The 6/8 coincidence status is not in sync when switching between 6/8 modes.) LOAD NOT MC (A master clear did not clear the PFC load status indication due to a partial load.) PFC VALID FORMAT (The PFC valid format code error status bits were incorrect.) NO BUSY STATUS (The maintenance busy status bit is not set.)

CARD EQUIPMENT TESTS

Mnemonic	Loading Mode	Parameters	Errors
CP1	Deadstart Binary, DSCL Binary Deck, ENS, Stand-Alone, Auto	Address 1500=Bit 0 Repeat subcondition Bit 1 Stop on error Bit 2 Stop at end of section Bit 3 Stop at end of test 1501=Bit 9 Repeat test Bit 10 Repeat section Bit 11 Repeat condition 1502=CCXE, channel and equipment 1503=Bit 0 Select ASCII option 1504=Special user pattern 1505=option† 1506=6681 select code 1507=Special user pattern option†	Messages Unformatted Messages Ccc 1111 2222 3333 4444 5555 6666 Compare error is detected. The card image is dumped six columns per message into the dayfile (cc=position of the first of the six columns). CP1 SECT0 NO COMPARE ERROR CARD XX CP1 SECT0, XX CARDS FOUND Formatted Messages Cpcce attt STssss Cdddd Ppppp cc = Card punch channel e = Card punch equipment a = BCD code in the first column of the title card for this section (A=1, B=2, etc.) t = Card type punched s = Last copied equipment status d = DCC/6681 status p = Location in the program where the error occurred

† Refer to publication number 60160600 for details regarding selection and entry of user pattern options.

Mnemonic	Loading Mode	Parameters	Errors
CP1 (Cont'd)		Address 1510=Bit 0 Check compare circuitry Bits 1-10 Select normal sections Bit 11 Enter user pattern	RES CHAN ACT CH ACT, Fffff (f=function) CH INACTIVE FULL OUT cc (c=decimal column output) NO DEACTIVE WAITING READY NO INT LINE COMP ERR EXT REJ F=ff RNB NOT CLR CH ACT NO ACTIVATE CHAN FULL CH EMPTY END SECTION INT NO STAT STAT EX Ssss EXT REJ CON NO IN RJ INT REJ TRANS PARITY NO EX RJ F=ff

Mnemonic	Loading Mode	Parameters	Errors
CR1	Deadstart Binary, DSCL Binary Deck, ENS, Stand-Alone, Auto	Address 1500=Bit 1 Stop on error Bit 2 Stop after next title card Bit 3 Stop after input tray empty 1501=Bit 9 Restart after input tray empty Bit 11 Repeat last I/O command 1502=CCXE, channel and equipment 1503=Bit 0 Select ASCII option 1506=6681 select code	Format A CRcce atttbi INFO nn Cww, EX xxxx, RCyyyy Data error detected on the last card input. c = Card reader channel e = Card reader equipment a = BCD code in column 1 of the title card for this section t = Pattern type b = Mode in which card was read (b=binary, c=BCD) i = Number representing method used to input the card: (0)-1400 select, 71 instruction, one word at a time (1)-1500 select, 71 instruction, one word at a time (2)-1400 select, 71 instruction, full card input (3)-1500 select, 71 instruction, full card input (4)-1400 select, 71 instruction, more than full card (5)-1500 select, 70 instruction, one word at a time

Mnemonic	Loading Mode	Parameters	Errors
CR1 (Cont'd)			n = Decimal number of errors found on this card w = Decimal word in which the first error was found x = Word expected y = Word received Formats B through I Crcce attt STssss Cdddd Ppppp msg c = Card reader channel e = Card reader equipment a = BCD code in the first column of the last read title card t = Card type s = Last copied equipment status p = Program error location d = 6681/DCC status msg = Unique element of each individual format, usually with error code (refer to publication no. 60160600) NOTE For a more detailed description of the following messages, refer to publication no. 60160600.

Mnemonic	Loading Mode	Parameters	Errors		
CR1 (Cont'd)			Error Code	Message Format	Message Description
			00	C	Running
			01	B	Reserved channel active
			02	B	Channel active
			03	G	Channel active after channel function ffff
			04	B	No activate
			05	B	Channel inactive
			06	B	Channel full
			07	B	Channel full after output
			10	F	Channel empty before inputting word ww
			11	B	Channel full after input
			12	B	No deactivate
			13	D	End of section
			14	E	End of test
			15	B	Waiting for ready status
			16	B	6681 interrupt but no equipment interrupt

Mnemonic	Loading Mode	Parameters	Errors		
CR1 (Cont'd)			Error Code	Message Format	Message Description
			17	B	Equipment interrupt but no 6681 interrupt
			20	B	No title card
			21	B	No file card
			22	1	Card out of sequence
			23	H	Status error
			24	B	Blank card
			25	B	External reject on function or connect
			26	B	Internal reject occurred
			27	B	Transmission parity error occurred
			30	B	No external reject on function
			31	B	No internal reject occurred
			32	B	No 7-9, binary cards
			33	B	7-9, no binary status
			34	B	Cannot read last card

DISK FILE TESTS

Mnemonic	Loading Mode	Parameters		Errors
DF7/ DF9	Stand-Alone, Auto	Address 1500=XXX1	Repeat subcondition	Messages
		=XXX2	Stop on error	Standard error messages have the following format.
		=XXX4	Stop at end of section	DF7 CXX Ey Uz SVVTW EEE XXXXXXXXXX-XXXXXXXXXX
		=XX1X	Stop at end of test	XX = Channel number y = Equipment number z = Unit number VV = Section W = Test (subsection)
		=XX2X	6681 mode I	EEE = Error code: 000-077 Select format A 100-177 Select format B 200-277 Select format C 300-377 Select format D 400-407 Select format E 410-477 Select format F
		1501=1XXX	Repeat test	
		=2XXX	Repeat section	
		=4XXX	Repeat condition	
		1502=CCEE	CC=channel and EE= equipment	

Mnemonic	Loading Mode	Parameters	Errors
DF7/ DF9 (Cont'd)		Address 1503=OUUU, unit selection (bit 0=unit 0, bit 1= unit 1, etc.) Bit 11=0 Run on non-buffered controller, 3553-1 Bit 11-1 Run on buffered controller, 3553-2 1504=LLLL, lower cylinder limit 1505=UUUU, upper cylinder limit 1506=2000, 6681 select code Bit 0 Section 12, track cross talk test Bit 1 Section 13, optional timing section Bit 2 Section 14, optional defective WLO track test	Format A: CHXXX EQXXXX Channel status and equipment status; used for abnormal channel or equipment status or connect and function rejects. Format B: EXYYYY ACYYYY Expected and actual equipment statuses; used when the action taken should result in a specific equipment status. Format C: ACCCCCHHSSEXCCCCHHSS Actual and expected disk address; used for return address errors. Format D: ACCCCCHHSS Disk address; used for data errors Format E: Blank; used for parameter selection errors.

Mnemonic	Loading Mode	Parameters	Errors
DF7/ DF9 (Cont'd)		Address 1507=Bit 3 Section 15, optional surface analysis =Bit 4 Section 16, optional quick surface check-checkword verify =Bit 5 Section 17, optional random read test =Bit 8 Section 20, parity test (CYBER 170 with 6681-F) =Bit 11 821 or 841, 0XXX-run 821 (normally selected), 4XXX-run 841 1510=SSSS, section selection (bit 0=section 0, bit 1=section 1, etc.) 1511=HH00, head selection 1512=CCCC, cylinder selection	Format F: OPXXX EXXXX ACXXXX TEST OPERAND EXPECTED 6681 STATUS ACTUAL 6681 STATUS Used in section 20 when parity testing should result in specific converter status. In addition to the standard message, a second line will be displayed: DF - BLXXXX Buffer Length TEXXXX Total Errors WDXXXX Word Failing EXXXX Expected Data ACXXXX Actual Data If bit 3 of parameter in location 1513 is set, this line will be displayed for each failing word in the buffer. **NOTE** Due to the number of error codes involved, refer to publication no. 60160600 for explanation of these error codes.

Mnemonic	Loading Mode	Parameters	Errors
DF7/ DF9 (Cont'd)		Address 1513 Bit 0 Stack 0 selection Bit 1 Stack 1 selection For 821 Bit 3 Set to ignore defect tracks Bits 4 and 5 Not used Bit 9 Even head For 841 Bit 3 Set to display all data errors in buffer Bit 9 Even head selection Bit 10 Odd head selection 1514=Seek count parameter for section 17 1515=Bit 0 Run short test if set Bit 1 Dump read and write buffers if set	

Mnemonic	Loading Mode	Parameters	Errors
DF7/ DF9 (Cont'd)		Address 1515=Bit 2 Use 7777 and 0000 in section 15 if bit is set. Use 5252 and 2525 if bit is clear. Bit 3 Random write/ read in section 17 if bit is set, read only if bit is clear. Bit 4 Report only one data error in S2T1 if bit is set. Report all data errors if bit is clear. Bit 5 Use standard patterns in S2T1 if bit is set. Use random pattern from clock if bit is clear.	

Mnemonic	Loading Mode	Parameters	Errors
DF7/DF9 (Cont'd)		Bit 8 Parity-enhanced 6681 (6681-F) must be set to run initial DCC and section 20 parity tests.	

DISPLAY TESTS

Mnemonic	Loading Mode	Parameters	Errors
DS1	DSCL Binary Deck, Dead-start Binary, ENS, Stand-Alone, Auto	Test loads and PS display appears on screen with the message ADDR. 1502=CC00 (CC=channel number). Type in 1502X CC00 (CR), space. Message ADDR. 1503=000U (U=console number). Type 1503X 000U (CR). Spacebar. The following parameters are displayed on the left screen. TEST - L=Left R=Right B=Both CHAR - Character desired for display SIZE - S=64 characters/line M=32 characters/line L=16 characters/line Library List A = Full alphabet, select tube, size C = Full screen, one character - select tube, character, size	Messages Select test from library list (A, C, D, I, S, X, or L). Incorrect or no test selected before depressing carriage return (Z is also correct selection). Channel errors are printed on line printer (parameters are at 1507 = CCEE).

Mnemonic	Loading Mode	Parameters	Errors
DS1 (Cont'd)		Library List (Cont'd) D = 32 by 32 dot roster, select tube I = 15 characters each size, select tube (20-millisecond rate) S = Single character, centered, select tube, character size X = Crossed diagonal lines, select tube L = Display all tests, select tube, character size Control CR = During control program, execute test. During L=display all tests, step to next test. BKSP = Correct typing error. BLANK = Erase all typed in code. SPACE BAR = During control program, drop program. During test from library, return to control program. Dot/character mode positioning comparison test may be selected by typing Z and selecting tube.	

Mnemonic	Loading Mode	Parameters	Errors
DS1 (Cont'd)		To repeat test, set 1501=1000. 1507=CCEE, channel and equipment of line printer for channel error printout.	

REMOTE TERMINAL TESTS

Mnemonic	Loading Mode	Parameters	Errors
RT3	Deadstart Binary, DSCL Card Deck, ENS, Stand-Alone, Auto	Address 1500=XXX2 Stop on error =XXX4 Stop at end of section =XX1X Stop at end of test 1501=1XXX Repeat test =2XXX Repeat section =4XXX Repeat condition 1502=CCEE, CC=channel, EE=equipment 1503=00XX If XX=00, program determines which DCSs it will test: =XXX1 Run test on DSC0 =XXX2 Run test on DSC1 =XXX4 Run test on DSC2 =XX1X Run test on DSC3	General Error Format CHaa EQb Sc DSCd eee Affff Egggg Phh aa = Channel number b = Equipment number c = Test section number (1 through 6) d = Data set controller number (0 through 3) eee = Error code ffff = Actual status or data gggg = Expected status or data hh = Pattern number (1 through 74) **NOTE** Because of error codes involved, refer to publication no. 60160600 for a detailed description of the error codes.

Mnemonic	Loading Mode	Parameters		Errors
RT3 (Cont'd)		Address 1504=000X	If X=1, 6674 tied through pass-on network of a 6681	
		1507=00AB	A=transmitting DSC number in section 2 and B=receiving DSC number in section 2 DSC number (section 6)	
		1510=00XX	Section flags:	
		=XXX1	Section 1, status check	
		=XXX2	Section 2, optional	
		=XXX4	Section 3, interrupt test	
		=XX1X	Section 4, data transfers	
		=XX2X	Section 5, multiplexed data transfers	
		=XX4X	Section 6, return transmissions from a remote terminal	

Mnemonic	Loading Mode	Parameters		Errors	
RT5	Stand-Alone, Auto	Address 1500=XXX1	Repeat condition	Messages	
		=XXX2	Stop on error	All error messages are prefixed by 6671 SX.	
		=XXX4	Stop at end of section	SX = Current section number	
		=XX1X	Stop at end of test	1CHRJ	Character reject set longer than character time during an output attempt
		1501=1XXX	Repeat test	2TNR	Terminal ready status was not set during an input or output operation.
		=2XXX	Repeat section	3MPER	Memory parity error status was set during an input or output operation.
		=4XXX	Repeat error	4VCNS	Valid character not set on input after one character time.
		=XXX1	Stop at beginning of section	5LD	Lost character status was set during an input operation.
		=XX1X	For 4800 baud MUX modification	6RESC	Receiver did not go into sync condition after four sync codes.
		=XX14	9600 baud, both bits must be set	7ABA	Channel was active before activate instruction.
		=XX2X	Will go to parameter stop on repeat test	10ABF	Channel was active before a function instruction.
		=X0XX	110 baud/11 bit if 103 mode is selected, MCP9=1XXX	11AAF	Channel was active after a function instruction.

Mnemonic	Loading Mode	Parameters		Errors	
RT5 (Cont'd)		Address 1501=X004	100 baud/8 ports	12AAD	Channel was active after a deactivate instruction.
		=X1XX	150 baud/10 bit if 103 mode is selected	13IAA	Channel was inactive after an activate instruction.
		=X2XX	300 baud/10 bit if 103 mode is selected	14LBD	Channel was inactive before deactivate instruction.
		=X3XX	134.5 baud/9 bit if 103 mode is selected		
		=X4XX	600 baud/10 bit if 103 mode is selected		
		=X5XX	1200 baud/10 bit if 103 mode is selected		
		1502=CCEE,	CC=channel, EE=equipment		
		1503=0000			
		1504=0001	Do not report memory parity errors; record number in location 1005		

Mnemonic	Loading Mode	Parameters		Errors
RT5 (Cont'd)		Address 1505=0000	Contains count of memory parity errors	
		1506=0000	Use normal 026 sync code	
		=0XXX	Sync code is not 026. With sync character 366, the MUX has been modified for no MPC. If location 1506 = 366, sections 7 and 17 will not be run by the software.	
		=4000	Transparent mode of operation	
		1507=0077	Bits 0 through 5, sections 14 through 21	
		Bit 6	TTY test	
		Bit 7	Utility routine	

Mnemonic	Loading Mode	Parameters	Errors
RT5 (Cont'd)		Address 1507=7XXX Number of extra bit times/ per character delay between transmit and receive 1510=XXXX Bits 2 through 11, sections 0 through 13 =0XXX 2000 baud, 201 mode 1511=1XXX 103 mode =2XXX 2400 baud, 201 mode =4XXX Full duplex, 201 mode =X777 Test terminal number Simulator or Echo Bit 8 = 0 and lower four bits give input and output terminal number.	

Mnemonic	Loading Mode	Parameters	Errors
RT5 (Cont'd)		Through Two Data Sets Bit 8=1 Bits 0 through 3 give output terminal number and bits 4 through 7 give the input terminal number.	
RT6	Stand-Alone, Auto	Address 1500=XXX2 Stop on error =XXX4 Stop at end of section =XX1X Stop at end of test 1501=1XXX Repeat test =2XXX Repeat section =4XXX Repeat condition =XXX1 Line mode 1502=CCEE, CC=channel, EE=equipment 1503=TTSS, TT=6671 channel number (00-17), SS=site address (60-77) This is the switch-selectable address of the 217 console. This ad-	Messages ERROR CHANNEL XX ACTIVE Channel XX failed to deactivate. CXX EX TXX SXX ERR EX XXXX REC XXXX C = Channel E = Equipment T = Terminal S = Site address EX = Expected REC = Received TERMINAL XX NOT READY MUX MEM PAR ERR MUX LOST DATA TERM XX LOST DATA TERM XX BAD SOM TERM XX BAD SIA TERM XX BAD STA, REXXX

Mnemonic	Loading Mode	Parameters	Errors
RT6 (Cont'd)		dress is 160_8 through 177_8 in the 217. Four switches at location B12 are used to select the 217 as site 00_8-17_8. The upper three bits are always set. The test uses six bits, of which the upper two must always be set. Address 1504=TTSS 1505=TTSS 1506=TTSS 1507=Bit 0 Line printer hammer bank test =Bit 1 Line printer wavy pattern test =Bit 2 Line printer format test =Bit 3 DCP memory test =Bit 4 Maintenance section =Bit 5 Paper tape punch test	TERM XX BAD MPC, REXXX TERM XX BAD EOM TERM XX BAD STA TO POLL, REXXX, EXXXX T XX NO SEND TERM XX NO RESPONSE TXX CHAR PAR ERR EXXX REC XXX CXX ERR SHOULD BE ACTIVE TXX ERR X TO X BCD EXP XX REC XX [Indicates terminal XX had error converting from (1) to (E) BCD or (E) to 1 BCD, expected XX, received XX.] SECTION 5 ERR SW TEST TERM XX RESPOND SEC5 TXX NO READ FROM ALERT TXX SEC6 ERR EXP XX REC XX TXX SEC6 ERR SHORT BATCH TXX CARD OUT OF SEQUENCE TXX INCORRECT E CODE TXX NO CAR DROP TXX RE POLL PAILED FUN NG TXX NO EOM CHAR REJ TIMEOUT TERM XX EOM, BUT NO MPC

Mnemonic	Loading Mode	Parameters	Errors
RT6 (Cont'd)		Address 1507=Bit 6 Paper tape reader test 1510=Bit 0 Control codes test =Bit 1 Display test =Bit 2 Display all H pattern =Bit 3 Keyboard test =Bit 4 INT/EXT BCD switch test =Bit 5 Error message enable/disable switch test =Bit 6 Attend/unattend switch test =Bit 7 Typewriter printer test =Bit 8 Card reader test =Bit 9 Line printer sliding alpha =Bit 10 Line printer variable buzzer = Bit 11 Line printer compress zeros and spaces	Ttt SEC15 ddd DATA ERR EXP eee REC rrr tt = Terminal number ddd = SEQ (sequential) or RAN (random) eee = Expected data rrr = Received data SHORT READ EOM AT FRAME nnn

Mnemonic	Loading Mode	Parameters	Errors
RTX	Stand-Alone, Auto	Address 1502=CCEE, CC=3266 channel, EE=3266 equipment 1503=XXYY, XX = odd unit (0-17) and YY = even unit (0-17) 1504=00CC, CC=communication channel for RT6 NOTE Refer to RT6 writeup for additional parameters. RT6 must be run in conjunction with this test.	Messages All error messages are displayed by RT6. Refer to RT6 writeup for error messages.
TT3	Deadstart Binary, DSCL Binary Deck, ENS, Stand-Alone, Auto	Address 1500=XXX1 Repeat condition =XXX2 Stop on error =XXX4 Stop at end of section =XX1X Stop at end of test	Messages Data ERR Axxxx Eyyyy ECz T=xxyy = Terminal pair that error occurred on xxxx = Actual character code received yyyy = Character code sent out z = Error code

Mnemonic	Loading Mode	Parameters	Errors
TT3 (Cont'd)		Address 1501=1XXX Repeat test =2XXX Repeat section =4XXX Repeat error condition 1502=CCEE, CC=channel, EE=equipment 1503=0000 1504=0000, normal character set (4000-IBM character set 134.5 baud, bit 0 of each 8-bit character set, character=bit 1 through 7, bit 0=stop bit) 1505=0000 1506=X177, character time in octal milliseconds; 103B=134.5 and 150 baud, 42B=300 baud, 21B=600 baud 1507=XXYY, XX=terminal out, YY=terminal in 1510=XX77, bits 0 (section 1) through 5 (section 6) 1511=0000	Error Code 1 Error occurred when disconnect code sent to terminal and input = nonzero. Error Code 2 Error occurred when the character code sent is not the same as the one received in the single character sequence. Error Code 3 Error occurred when the character code sent is not the same as the one received in the stacked sequence. SERVICE FAILURE DID NOT CLR SERVICE FAILURE NOT SET LOST DATA DID NOT SET NO CHARACTER REJECT TERMINAL NOT READY CHARACTER REJECTED LOST DATA ON READ VALID CHAR NOT SET

Mnemonic	Loading Mode	Parameters	Errors
TT3 (Cont'd)			ABA Channel was active before an activate instruction. ABF Channel was active before a function instruction. AAF Channel was active after a function instruction. AAD Channel was active after a deactivate instruction. IAA Channel was inactive after an activate instruction. IBD Channel was inactive before a deactivate instruction.
TT5	Deadstart Binary, Stand-Alone, Auto	Address 1503=3266 connect code: First octal digit = MPX channel number Second octal digit = 0 if section A, 1 if section B Third octal digit = Always 1 (MPX decoder plug) Fourth octal digit = MPX equipment number	Displays Error On No Lost Character Communication Break Error On Char Req Error On No Char Ready Data Compare Error - EPX=XXX, ACT=XXX, CHAN=X Error On Lost Character Transmission Parity Error Fnc Transmission Parity Error Data External Reject E=00, CH=00 Internal Reject E=00, CH=00

Mnemonic	Loading Mode	Parameters	Errors
TT5 (Cont'd)		Address 1504=Section flags: Bit 0 = Section 1, interrupts test Bit 1 = Section 2, echo test Bit 2 = Section 3, lost character Bit 3 = Section 4, full line of each character Bit 4 = Section 5, Teletype input test Bit 5 = Section 6, RY pattern	

CYBER 170 STM TESTS

KEYBOARD COMMANDS

STM AND UTL

Keyboard Entries

All entries except the following single key commands terminate with carriage return.

Single Key Commands

+	Roll display forward
-	Roll display back
left blank	Erase keyboard buffer
right blank	Set repeat mode
backspace	Erase last character typed in

Basic Commands

Parameters enclosed in ( ) are optional.
A comma , or spacebar separates parameters.
Leading zeros are not required on octal parameters.

Select PPM Command

PP, N	Selects PP N for DP, WP, and commands

Display Commands

DP, XXXX(, N)	Display selected PP (N) memory from XXXX.
DC, XXXXXX	Display central memory from XXXXXX.
XP, XXXXXX	Display exchange packages at CM LOCATION XXXXXX and XXXXXX+20B.
DS	Select status register display (STM only).
PA	Select parameter display (STM only).

Data Entry Commands

WP, XXXX, AAAA (, BBBB, CCCC, DDDD, EEEE)	Write AA-EE into selected consecutive PPM addresses, starting at XXXX.
WC, XXXXXX, N, AAAA(, BBBB, CCCC, DDDD, EEE)	Write AAAA-EEEE into CM address XXXXXX, N; starting byte is 0 to 4.

In all data entry commands, a + instead of a, as the first separater causes the address to be sequentially incremented by number of bytes entered.

Status Register Commands

OF, C1(, C2, C3, C4)
ON, C1(, C2, C3, C4)

Deselects/selects status monitoring by STM for the following codes.

U0	CPU 0 stop
U1	CPU 1 stop
P0	PPS 0 memory errors
C0	PPS 0 channel parity errors
P1	PPS 1 memory parity errors
C1	PPS 1 channel parity errors
XU	Transmission parity errors detected by CPU
XC	Transmission parity errors detected by CSC
XS	Transmission parity errors detected by CSU
X0	Transmission parity errors detected by PPS 0
X1	Transmission parity errors detected by PPS 1
SC	SECDED errors
EC	ECS coupler parity errors
S0	PPS 0 detected double SECDED error
S1	PPS 1 detected double SECDED error
AL	All of the above
CH	Read and display chip select on SECDED errors

NOTE

For machines containing ECO CA 037722, any time SECDED errors are deactivated from monitoring (SC in the above table), S0 and/or S1 must be deactivated.

MR, LOCK(, ON)	Enables lock on the status register error. (Does not clear SCR error bit and will cease displaying any other error message.)
MR, LOCK, OFF	Disables lock on the status register error.
MR, CLR	Clears currently locked-on error.
SR, 2X	Sets/clears double speed bit for all PPUs in the system.
CR, 2X	
SR, DS, N	Sets P register display mode for PP N.
CR, DS	Clears P register display mode.
SR, NM(, X)	Sets PP selection mode to manual of PPS X.
CR, MN(, X)	Clears manual PP selection mode (sets program mode).
SR, FE, N	Forces exit PP N.
SR, FD, N	Forces deadstart PP N.
SR, C5(, X)	Toggles C5 full signal of PPS X.
SR, CB(, X)	Toggles clear central busy of PPS X.
SR, ZP	Sets/clears force zero parity bit according to the following parameters.
CR, ZP	
, PM(, X)	PPS X PPM
, SC	SECDED code and data from CMC to PPS
, PA(, X)	PPS X to CMC address
, PD(, X)	PPS X to CMC data
, IO(, X)	I/O channels of PPS X
, UA	CMC to CSU address
, AX	CPU X to CMC address (X is 0)
, DX	CPU X to CMC data (X is 0)
SR, IS	Inhibits SECDED reporting.
CR, IS	Enables SECDED reporting.
SR, PE	Sets stop on PPM parity error.
CR, PE	Clears stop on PPM PE.
SR, BT, ZZZ(, X)	Sets bit ZZZ in PPS X SCR.
CR, BT, ZZZ(, X)	Clears bit ZZZ in PPS X SCR.
CR, ALL(, X)	Clears all bits of PPS X SCR.

SR, FM, Z	Sets frequency margin according to Z. Z is 0 to 7.
CR, FM	Clears frequency margin.
SR, RF, LO	Sets refresh margin low/high.
SR, RF, HI	
CR, RF	Clears refresh margin.

STM Commands to Control Tests

Backspace	Stops test.
Spacebar	Continues test.
R	Restarts test.
PA, N, AAAA (, BBBB, CCCC, DDDD, EEEE)	Enters parameters AA-EE into N, N+1, N+2 etc.
FL, XX(, YY, ZZC, WWC)	Activates flags XX and YY. Deactivates flags ZZ and WW. Test flags are:

SE	Stop on error
SC	Stop end of condition
SS	Stop end of section
ST	Stop end of test
SM	SCOPE mode
AE	Abort error checking
RC	Repeat condition
RS	Repeat section
RT	Repeat test

B<, XXXX	Breakpoint software at address XXXX.

Utility Commands

G XXXX	Executes user program in selected PP at address X.
S	Stops user program. User programs can be keyed into all PPMs other than the ones in which STM (test running under control of STM) or UTL is residing in.

The following rules must be adhered to.

1. To maintain communication with the monitor, execute an RJM to location 7701B.
2. To stop the program, do an LJM to location 7710B.
3. The program must not use low core 0 to 5 and high core 7700B to 7777B.

4. While the program is running, the PPM can be displayed. To write into the PPM, the program must be stopped.

PT, N, XXXX, YYYY, AAAA(, BBBB, CCCC, DDDD, EEEE)	Fills PPM N with PTRN AA-EE from XXXX to YYYY-1.
PT, CM, XXXXXX, YYYYYY, AAAA (, BBBB, CCCC, DDDD, EEEE)	Fills CM with pattern AA-EE from XXXXXX to YYYYYY-1.
MO, M, N, XXXX, YYYY, ZZZZ	Moves data in PPM M from addresses XXXX to YYYY-1 to PPM N address ZZZZ.
SCRX, YZZZ	Does function Y on word/bit ZZZ in SCR of PPS X.

MTR

OF, C1(, C2, C3, C4)	Same as STM.
ON, C1(, C2, C3, C4)	
MR, LOCK(, ON).	Enables lock on the status register error. (Does not clear SCR error bit and will cease displaying any other error message.)
MR, LOCK, OFF.	Disables lock on the status register error.
MR, LOCK, P1, X.	Sets lock-on error recorded by bit P1 of SCR X.
MR, CLR.	Clears currently locked-on error.
MR, INIT.	Initializes error counts.
MR, DROP.	Drops MTR.
MR, EXCH, P1.	MTR exchanges CPU(P1). If CPU(P1) had stopped on a breakpoint, it is restarted at breakpoint address +1.
SR, 2X.	Same as STM.
CR, 2X.	
SR, DS, N.	Same as STM.
CR, DS.	
SR, MN(, X).	Same as STM.
CR, MN(, X).	
SR, FE, N.	Same as STM.
SR, FD, N.	
SR, C5(, X).	Same as STM.
SR, CB(, X).	
SR, ZP, XX	Same as STM.
CR, ZP, XX	
SR, IS.	Same as STM.
CR, IS.	
SR, PE.	Same as STM.

CR, PE.	
SR, BT, ZZZ(, X).	Same as STM.
CR, BT, ZZZ(, X).	
CR, AL(, X).	
SR, FM, Z.	Same as STM.
CR, FM.	
SR, RF, HI.	Same as STM.
SR, RF, LO.	
CR, RF.	
SR, MA, P1, P2, P3.	Sets voltage margin type and scan frequency.
SR, MQ, P1, P2, P3.	Scans reference voltage margins on quadrants P1 to P2, checking P3 for response.
SR, MS, P1, P2, P3, P4.	Scans reference voltage margins on modules P2 to P3 of all quadrants P1 simultaneously, checking P4 for response.
SR, VS, P1, P2, P3.	Uses P1 first sequence reference voltage margin, P2 second-sequence reference voltage margin, and scan time P3 to scan reference voltage margins.
SR, BH, P1.	Cycles low- and high-reference voltage margins sequentially to all modules of quadrants P1.
SR, CW, NR.	
SR, LW, WD.	Sets clock pulse width to narrow/wide.
CR, CW.	Clears clock pulse width.

BP, XXXXXX, ZZ. Sets breakpoint at address XXXXXX function ZZ.

CZ	From CPU port
PZ	From PPU port
AZ	From both ports
ZR	For read only
ZW	For write only
Z1	For RNI only
ZA	For all

BP,. Clears breakpoint.

MCLR. Master clears CSUs and CPUs.

STANDARD PARAMETERS

PPU Tests

Parameter words 2 to 7 are preset according to the SYBBB, XXX, Y, Z entry to CEL.

```
Word 00 Bit 0 = 1   SCOPE mode
        Bit 1 = 1   Stop on error
        Bit 2 = 1   Stop at end of each section
        Bit 3 = 1   Stop at end of test
        Bit 4 = 1   Abort error checking
        Bit 5 = 1   Stop at end of each condition
     01 Bit 9 = 1   Repeat test
        Bit 10= 1   Repeat section
        Bit 11= 1   Repeat condition
     02 Bit 0 = 1   Test CPU0
        Bit 1 = 1   Test CPU1
        Bit 2 = 1   CPU is a CDC CYBER 175
        Bit 3 = 1   Test CSU0
        Bit 4 = 1   Test CSU1
        Bit 6 = 1   Test PPS0
        Bit 7 = 1   Test PPS1
     04             PPUS to be tested in PPS0
        Bit 0 = 1   Test PPU0
        Bit 1 = 1   Not used
     05             PPUs to be tested in PPS1
     06             Channels to be tested in PPS0
        Bit 0 = 1   Test channel 0
        Bit 1 = 1   Test channel 1
     07             Channels to be tested in PPS1
     10 through 12 Section flags
        Bit 0 of 10 = 1   Section 0
        Bit 1 of 10 = 1   Section 1
```

CPU Tests

Address 3, 4	Not used	
5	X XXX XXX XX1	Loop on failure
	X XXX XXX X1X	Stop on error
	X XXX XXX 1XX	Stop at end of section
	X XXX XX1 XXX	Stop at end of test
	X XXX X1X XXX	Repeat section
	X XXX 1XX XXX	Repeat test
	X X1X XXX XXX	Repeat condition
	X 1XX XXX XXX	Stop at end of condition
	1 XXX XXX XXX	Abort error checking
6	Section flags	
7	000...000	Use program supplied seed or use XXX...XXX as seed for random number generator.
	XXX...XXX	

PPM

Word 14 = OOTT	TT is the number of test resident PPU.
15 = UUUU	UUUU is the lower limit of PP memory to be tested.
16 = VVVV	VVVV is the upper limit of PP memory to be tested.
17 = ZZZZ	ZZZZ is number of write cycles.
20 = YYYY	YYYY is number of read cycles.
21 = XWWW	WWW is size of delay.

Bit	
0 through 8	Specify the delay count for the refresh section.
9 = 1	Count is in milliseconds.
10 = 1	Count is in seconds.
11 = 1	Count is in minutes.

Display No.	Display Format
0	QUICK LOOK TESTING PPU XX ADDRESS XXXX EXP DATA XXXX REC DATA XXXX

Display No.	Display Format
1	PPU SELECTION TEST TESTING PPU XX ADDRESS XXXX EXP DATA XXXX REC DATA XXXX
2	REFRESH TEST TESTING PPU XX ADDRESS XXXX EXP DATA XXXX REC DATA XXXX
3	PARITY TEST TESTING PPU XX PARITY FORCED TO ZERO YES/NO EXPECTED PARITY ERROR YES/NO RECEIVED PARITY ERROR YES/NO ADDRESS XXXX PATTERN XXXX
4	ADDRESS TEST ASC. ORDER/DESC. ORDER TESTING PPU XX ADDRESS XXXX EXP DATA XXXX REC DATA XXXX
5	STANDARD/RANDOM PATTERNS TEST TESTING PPU XX ADDRESS XXXX EXP DATA XXXX REC DATA XXXX
6	RANDOM ADDRESS TEST TESTING PPU XX ADDRESS XXXX EXP DATA XXXX REC DATA XXXX

CSP

Word 13 = XXYY YYYYYY is the lower limit of
14 = YYYY central memory to be tested.
15 = XXZZ ZZZZZZ is the upper limit of
16 = ZZZZ central memory to be tested.
17 = Bit 0=1 Loop on CM read
Bit 1=1 Loop on CM write
Bits 0 and 1=1 Loop on CM write followed by CM read
20 = Bit 0=0 Normal operation
Bit 0=1 CSI mode
21 = XWWWW WWW is size of delay.

	Bits	
	0 through 8	Delay count for the refresh test section.
	9 = 1	Count is in milliseconds.
	10 = 1	Count is in seconds.
	11 = 1	Count is in minutes.
22 = SSSS		SSSS is the seed for the pseudo-random number generator.
23 = 0		Run sections 1 and 2 in block mode.
= 1		Run sections 1 and 2 in bank mode.
24 = OOAA		AA is the lower CSU, quad, and bank limit in bank mode.
25 = OOBB		BB is the upper CSU, quad, and bank limit in bank mode.
26 Bit 0 = 1		Do not check for XMSN P.E.
Bit 1 = 1		Do not check for SECDED errors.

Displays

Parity Errors

```
     SECTION TITLE
             BLANK
( ON WRITE )          ( CSC ADDR PE )
( ON READ  )          ( CSC DATA PE )
                      ( CSU ADDR PE )
                      ( MEM FAULT   )

CSU XX QUAD XX CHIP XX BANK XX
ADDRESS XXXXXX
          ( BLOCK TRANSFER )
          ( WORD TRANSFER  )


EXP DATA  XXXX XXXX XXXX XXXX XXXX
 REC DATA  XXXX XXXX XXXX XXXX XXXX
```

SECDED and Compare Errors

```
     SECTION TITLE
             BLANK
          ( COMPARE  ERROR )
          ( SINGLE     ERROR )
          ( MULTIPLE ERROR )
CSU XX QUAD XX CHIP XX BANK XX
BIT XXXX MODULE SLOT (ROW) (COLUMN)
 SYND XX ARRAY XXX
ADDRESS XXXXXX
EXP DATA XXXX XXXX XXXX XXXX XXXX
REC DATA XXXX XXXX XXXX XXXX XXXX
```

```
( BLOCK TRANSFER )
( WORD TRANSFER  )
```

History Table

```
        SECTION TITLE
              BLANK
ADDRES   SC SA          EXP DATA
XXXXXX XXX XX XXXXXXXXXXXXXXXXXXXX

         REC DATA              SE-DE
 XXXXXXXXXXXXXXXXXXXX          S/D
```

SCR

Word 13 = Breakpoint test mode
Bit 0 = 0 Write mode only
= 1 Read and write mode

Displays

Error Display 0

```
Line 00     CLEAR/TEST/SET BIT
     01     TEST ON PPS XX SCR
     02
     03     SCR BIT XXXX FAILED (OK)
     04
     05     CODE OX
            (CLEAR BIT TEST BIT - CODE 01)
            (SET     BIT TEST BIT - CODE 02)
            (CLEAR BIT TEST BIT - CODE 03)
```

Error Display 1

```
Line 00     CLEAR ALL
     01     TEST ON PSS XX SCR
     02
     03     SCR BIT XXXX FAILED (OK)
     04
     05     CODE 1X
            (CLEAR BIT TEST BIT - CODE 11)
            (SET     BIT TEST BIT - CODE 12)
            (CLEAR ALL TEST BIT- CODE 13)
```

Error Display 2

```
Line 00     TEST * SET BIT
     01     TEST ON PPS XX SCR
     02
     03     SCR BIT XXXX FAILED (OK)
     04
     05     CODE 2X
            (CLEAR BIT TEST AND SET BIT -
              CODE 21)
            (TEST BIT                    -
              CODE 22)
```

Error Display 3

```
Line 00     TEST * CLEAR BIT
     01     TEST ON PPS XX SCR
     02
     03     SCR BIT XXXX FAILED (OK)
     04
     05     CODE 3X
            (SET BIT TEST AND CLEAR BIT -
              CODE 31)
            (TEST BIT                    -
              CODE 32)
```

Error Display 4

```
Line 00     BIT ADDRESSING
     01     TEST ON PPS XX SCR
     02            USES *BIT* CMDS
     03     TESTING BIT XXXX GOING UP (DOWN)
     04              60    44    30    14   00
     05     EXPCTD  XXXX XXXX XXXX XXXX
                    XXXX
     06     ACTUAL  XXXX XXXX XXXX XXXX
                    XXXX
            LINES 7 THROUGH 17B ARE SIMILAR
            TO LINES 4 THROUGH 6.
```

Error Display 5

```
Line 00     READ WORD
     01     TEST ON PPS XX SCR
     02            USES READ WORD CMD
     03     TESTING WORD XXXX
     04              60    44    30    14   00
     05     EXPCTD  XXXX XXXX XXXX XXXX
                    XXXX
     06     ACTUAL  XXXX XXXX XXXX XXXX
                    XXXX
            LINES 7 THROUGH 17B ARE SIMILAR
            TO LINES 4 THROUGH 6.
```

Error Display 6

```
Line 00     TEST ALL
     01     TEST ON PPS XX SCR
     02
     03     SCR BIT XXXX FAILED (OK)
     04
     05     CODE 6X
            (CLEAR ALL TEST ALL - CODE 61)
            (SET    BIT  TEST ALL - CODE 62)
```

Error Display 7

```
Line 00     2X PP SPEED
     01     TEST ON PPS XX SCR
     02
     03     TEST ON PP XX FAILED (OK)
            SCR BITS TESTED OR USED
            BIT 124B - PPS 2X SPEED MODE
            BIT 170B - PP SELECT CODE BIT 0
            BIT 171B - PP SELECT CODE BIT 1
            BIT 172B - PP SELECT CODE BIT 2
            BIT 173B - PP SELECT CODE BIT 3
            BIT 174B - PP SELECT AUTO/MANUAL
                       MODE
```

Error Display 10

An error display occurs either if the channel does not become active or if the A register count is not 10000B.

```
Line 00     PP DEAD-START
     01     TEST ON PPS XX SCR
     02
     03     TEST ON PP XX FAILED (OK)
            SCR BITS TESTED OR USED
            BIT 170B - PP SELECT CODE BIT 0
            BIT 171B - PP SELECT CODE BIT 1
            BIT 172B - PP SELECT CODE BIT 2
            BIT 173B - PP SELECT CODE BIT 3
            BIT 174B - PP SELECT AUTO/MANUAL
                       MODE
            BIT 176B - FORCE PP DEADSTART
```

Error Display 11

```
Line 00     I/O CMD Q5 BIT
     01     TEST ON PPS XX SCR
     02
     03     TEST ON PP XX FAILED (OK)
            SCR BITS TESTED OR USED
            BIT 170B - PP SELECT CODE BIT 0
            BIT 171B - PP SELECT CODE BIT 1
            BIT 172B - PP SELECT CODE BIT 2
            BIT 173B - PP SELECT CODE BIT 3
            BIT 174B - PP SELECT AUTO/MANUAL
                       MODE
            BIT 176B - FORCE PP DEADSTART
```

Error Display 12

```
Line 00     FORCE EXIT
     01     TEST ON PPS XX SCR
     02
     03     TEST ON PP XX FAILED (OK)
            SCR BITS TESTED OR USED
            BIT 170B - PP SELECT CODE BIT 0
            BIT 171B - PP SELECT CODE BIT 1
            BIT 172B - PP SELECT CODE BIT 2
            BIT 173B - PP SELECT CODE BIT 3
            BIT 174B - PP SELECT AUTO/MANUAL
                       MODE
            BIT 175B - FORCE EXIT
            BIT 176B - FORCE PP DEADSTART
```

Error Display 13

Assuming the breakpoint comparator failed and the displayed addresses are different, a match occurred on unlike addresses. If the addresses are the same, no match occurred when a match should have occurred.

```
Line 00     BKPT COMPARATOR
     01     TEST ON PPS 00 SCR
     02
     03
     04     BKPT COMPARATOR FAILED (OK)
     05
     06     BKPT ADRS     XXXXXX
     07     MEMORY ADRS XXXXXX
```

Error Display 14

An error display is made if any one of the five different expected and actual value pairs are not in agreement.

```
Line 00     BKPT P-REG/PP CODE
     01     TEST ON PPS XX SCR
     02
     03
     04                          EXPCTD ACTUAL
     05
     06     MATCH BIT              01     XX
     07     PP BKPT BIT            01     XX
     10     PORT SEL BITS          XX     XX
     11     P-REG BITS           XXXX   XXXX
     12     PP CODE BITS           XX     XX
```

Error Display 15

NUL indicates that no match occurred, which would be correct if RNI was selected.

```
Line 00      BKPT FUNCTION
     01      TEST ON PPS XX SCR
     02
     03
     04      BKPT FUNCTION FAILED (OK)
     05
     06      SELCTD  XXXX  (READ, WRITE, RNI,
                            ALL)
     07      EXCUTD  XXXX  (READ, WRITE)
     10      SENSED  XXXX  (READ, WRITE, RNI,
                            EXCH, NUL)
```

SCD

Word 13B = XXYY	YYYYYY is the central memory
14B = YYYY	address to be used for testing.
15B = 0000	If nonzero, test all memory available according to parameter 3 (used by section 3 only).
16B ≠ 0000	SCR contains chip select upon detection of SECDED error.

NOTE

If ECO CA 037722 has been installed, refer to publication no. 60409500.

Displays

Error Display 0

```
Line 00                    TITLE
     01                    BLANK
     02      ADDR TESTED  XXXXXX
     03                      48     36     24
     04      EXP DATA     XXXX XXXX XXXX
                                12     0
                            XXXX XXXX
     05      REC DATA     XXXX XXXX XXXX
                            XXXX XXXX
     06      EXP SYND     XXXX
     07      REC SYND     XXXX
     08      EXP ARRAY    XXXX CH Y
     09      REC ARRAY    XXXX CH Y
     10      EXP SINGLE ERROR
     11      REC (SINGLE/DOUBLE/NO) ERROR
     12      FORCE ZERO SECDED CODE WAS ON
     13      BIT TESTED   XXXX
```

Error Display 1

```
Line 00     * SCD01 - SINGLE ERROR CORREC-
              TION 1 TO 0*
     01                BLANK
     02     ADDR TESTED  XXXXXX
     03                     48     36     24
     04     EXP DATA      0020   1403   0060
     05     REC DATA      XXXX XXXX XXXX
                             12     0
                           1403   0040
                          XXXX XXXX
     06     EXP SYND      0000
     07     REC SYND      XXXX
     08     EXP ARRAY     0000   C H Y
     09     REC ARRAY     XXXX C H Y
     10     EXP NO ERROR
     11     REC (SINGLE/DOUBLE/NO) ERROR
     12     FORCE ZERO SECDED CODE WAS ON
```

Error Display 2

```
Line 01     *SCD02 - DOUBLE ERROR DETECTION
              TEST*
     01                BLANK
     02     ADDR TESTED  XXXXXX
     03                     48     36     24
     04     EXP DATA      XXXX XXXX XXXX
                             12     0
                           XXXX XXXX
     05     REC DATA      XXXX XXXX XXXX
                          XXXX XXXX
     06     EXP SYND      XXXX
     07     REC SYND      XXXX
     08     EXP ARRAY     XXXX C H Y
     09     REC ARRAY     XXXX C H Y
     10     EXP DOUBLE ERROR
     11     REC (SINGLE/DOUBLE/NO) ERROR
     12     FORCE ZERO SECDED CODE WAS ON
```

Error Display 3

```
Line 00     *SCD03 - CODE BIT SINGLE ERROR
              DETECTION*
     01                BLANK
     02     ADDR TESTED  XXXXXX
     03                     48     36     24
     04     EXP DATA      XXXX XXXX XXXX
                             12     0
                           XXXX XXXX
     05     REC DATA      XXXX XXXX XXXX
                          XXXX XXXX
     06     EXP SYND      XXXX
     07     REC SYND      XXXX
     08     EXP ARRAY     XXXX C H Y
```

```
09      REC ARRAY     XXXX C H Y
10      EXP SINGLE ERROR
11      REC (SINGLE/DOUBLE/NO) ERROR
12      FORCE ZERO SECDED CODE WAS ON
```

Error Display 4

```
Line 00     *SCD04 - ARRAY ADDR REPORT ON
              ERROR TEST*
01                  BLANK
02          ADDR TESTED  XXXXXX
03                          48     36     24
04          EXP DATA      0000   0000   0000
05          REC DATA      XXXX XXXX XXXX
                             12      0
                           0000   0000
                           XXXX XXXX
06          EXP SYND      0377
07          REC SYND      XXXX
08          EXP ARRAY     XXXX C H Y
09          REC ARRAY     XXXX C H Y
10          EXP DOUBLE ERROR
11          REC (SINGLE/DOUBLE/NO) ERROR
12          FORCE ZERO SECDED CODE WAS ON
```

Error Display 5

```
Line 00     *SCD05 - CSC TO XMISSION PATH
              TEST*
01                  BLANK
02          ADDR TESTED  XXXXXX
03                          48     36     24
04          EXP DATA      XXXX XXXX XXXX
                             12      0
                           XXXX XXXX
05          REC DATA      XXXX XXXX XXXX
                           XXXX XXXX
06          EXP SYND      0000
07          REC SYND      XXXX
08          EXP ARRAY     0000   C H Y
09          REC ARRAY     XXXX   C H Y
10          EXP NO ERROR
11          REC (SINGLE/DOUBLE/NO) ERROR
12          FORCE ZERO SECDED CODE WAS OFF
```

NOTE

The following displays always appear with the monitor header portion.

Error Display 6

Line

```
 0       PP STOP ON DBL ERR TEST
 1       TESTING PPXX
 2       STOP ON DBL ERR WAS (ON)
                             (OFF)
 3       PPXX EXP (A) STOP ON DBL ERR
                 (NO)
 4       PPXX REC (A) STOP ON DBL ERR
                 (NO)
 5       PP PORT EXP A DBL ERR
 6       PP PORT REC (A)
                     (NO) DBL ERR
 7       PP NUMBER   2      11   20          31
 8       EXP STATUS  XXXXXXXX XXXXXXXXXX
 9       REC STATUS  XXXXXXXX XXXXXXXXXX
10       PPS-0 SCR BITS 16-27 EXP *XXXX
11       PPS-0 SCR BITS 16-17 REC *XXXX
12       PPS-1 SCR BITS 16-27 EXP *XXXX
13       PPS-1 SCR BITS 16-27 REC *XXXX

         DEPENDING ON ERROR TYPE
         THE DISPLAY WILL BE :-

         LINES 0-4     OR
         LINES 0-6     OR
         LINES 0-9     OR
         LINES 0-11    OR
         LINES 0-13
```

Error Display 7

Line

```
 0       INHIBIT SNG ERR TEST
 1
 2       INHIBIT SNG ERR WAS (ON)
                             (OFF)
 3       EXP (SNG) ERR
              (DBL)
              (NO)
 4       REC (SNG) ERR
              (DBL)
              (NO)
 5       EXP PPS-0 SCR BIT 3 (ON)
                             (OFF)

         DEPENDING ON ERROR TYPE
         DISPLAY WILL BE :-

         LINES 0, 1, 2, 3, 4 OR
         LINES 0, 1, 2, 3, 4, 5, 6.
```

TRC

Displays

Error Display 0

```
Line 00     *CSU-CPU DATA XMISS PATH TEST*
     01     ERROR EXIT BIT 53 TEST
     02
     03     FORCE ZERO PARITY     ON/OFF
     04     PARITY ERR EXP        YES/NO
     05     PARITY ERR REC        YES/NO
     06     ERR MODE SELECTED     YES/NO
     07     ERR EXIT BIT SET      YES/NO
     08     EXP RA0       XX XX XXXXXX
     09     REC RA0       XX XX XXXXXX
     10     EXP CPU RESPONSE
              RUNNING/STOPPED
     11     REC CPU RESPONSE
              RUNNING/STOPPED
     12     COMPARE DATA ERR
     13     EXP DATA      XXXX XXXX XXXX
                            XXXX XXXX
     14     REC DATA      XXXX XXXX XXXX
                            XXXX XXXX
```

Error Display 1

```
Line 00     *ERROR EXIT TEST ON SECDED ERR*
     01     ERROR EXIT BIT 53 TEST
     02
     03     FORCE ZERO SECDED ON
     04     SECDED ERR REC        YES/NO
     05     DOUBLE ERR EXP        YES
     06     DOUBLE ERR REC        YES/NO
     07     ERR MODE SELECTED     YES/NO
     08     ERR EXIT BIT SET      YES/NO
     09     EXP RA0       XX XX XXXXXX
     10     REC RA0       XX XX XXXXXX
     11     EXP CPU RESPONSE
              RUNNING/STOPPED
     12     REC CPU RESPONSE
              RUNNING/STOPPED
     13     COMPARE DATA ERR
     14     EXP DATA      XXXX XXXX XXXX
                            XXXX XXXX
     15     REC DATA      XXXX XXXX XXXX
                            XXXX XXXX
```

Error Display 2

```
Line 00     *ERROR EXIT TEST ON CSU ADR PE*
     01     ERROR EXIT BIT 52 TEST
     02
     03     FORCE ZERO PARITY    ON/OFF
     04     PARITY ERR EXP       YES/NO
     05     PARITY ERR REC       YES/NO
     06     ADDRESS       XXXXXX
     07     ERR MODE SELECTED  YES/NO
     08     ERR EXIT BIT SET     YES/NO
     09     EXP RA100   XX XX XXXXXX
     10     REC RA100   XX XX XXXXXX
     11     EXP CPU RESPONSE
              RUNNING/STOPPED
     12     REC CPU RESPONSE
              RUNNING/STOPPED
```

Error Display 3

```
Line 00     *CPU-CMC DATA XMISS PATH TEST*
     01     ERROR EXIT BIT 52 TEST
     02
     03     FORCE ZERO PARITY    ON/OFF
     04     PARITY ERR EXP       YES/NO
     05     PARITY ERR REC       YES/NO
     06     ERR MODE SELECTED  YES/NO
     07     ERR EXIT BIT SET     YES/NO
     08     EXP RA0     XX XX XXXXXX
     09     REC RA0     XX XX XXXXXX
     10     EXP CPU RESPONSE
              RUNNING/STOPPED
     11     REC CPU RESPONSE
              RUNNING/STOPPED
     12     COMPARE DATA ERROR
     13     EXP DATA      XXXX XXXX XXXX
                            XXXX XXXX
     14     REC DATA      XXXX XXXX XXXX
                            XXXX XXXX
```

Error Display 4

```
Line 00     *CPU-CMC ADDR XMISS PATH TEST*
     01     ERROR EXIT BIT 52 TEST
     02
     03     FORCE ZERO PARITY    ON/OFF
     04     PARITY ERR EXP       YES/NO
     05     PARITY ERR REC       YES/NO
     06     ADDRESS       XXXXXX
     07     ERR MODE SELECTED  YES/NO
     08     ERR EXIT BIT SET     YES/NO
     09     EXP RA1     XX XX XXXXXX
     10     REC RA1     XX XX XXXXXX
     11     EXP CPU RESPONSE
              RUNNING/STOPPED
     12     REC CPU RESPONSE
              RUNNING/STOPPED
```

TRP

Word 13B = XXYY YYYYYY is the central memory
     14B =   test address.

Displays

Error Display 0

```
Line 00    *TR. 00 PPS-CMC ADDR PATH
             XMISSION TEST*
     01              BLANK
     02    ADDR XXXXXX
     03    PE EXPECTED (CMC ADDR/NONE)
     04    PE RECEIVED (CMC ADDR/NONE)
     05    FORCE ZERO PARITY (ON/OFF)
```

Error Display 1

```
Line 00    *TR. 01 PPS-CMC DATA PATH
             XMISSION TEST*
     01              BLANK
     02    ADDR XXXX
     03    PE EXPECTED (CMC DATA/NONE)
     04    PE RECEIVED (CMC DATA/NONE)
     05    FORCE ZERO PARITY (ON/OFF)
     06    DATA EXP      XXXX XXXX XXXX
                           XXXX XXXX
```

Error Display 2

```
Line 00    *TR. 02 CMC-CSU ADDR PATH
             XMISSION TEST*
     01              BLANK
     02    ADDR XXXXXX
     03    PE EXPECTED (CSU ADDR/NONE)
     04    PE RECEIVED (CSU ADDR/NONE)
     05    FORCE ZERO PARITY (ON/OFF)
```

Error Display 3

```
Line 00    *TR. 03 CMC-PPS DATA PATH
             XMISSION TEST*
     01              BLANK
     02    ADDR XXXXXX
     03    PE EXPECTED (PYR DATA/NONE)
     04    PE RECEIVED (PYR DATA/NONE)
     05    FORCE ZERO PARITY (ON/OFF)
     06    DATA EXP      XXXX XXXX XXXX
                           XXXX XXXX
     07    DATA REC      XXXX XXXX XXXX
                           XXXX XXXX
     08    NO PP PARITY (MOD C)
```

Error Display 4

Displayed only if wrong parity error is received.

Line 00	*TR. 04 WRITE LOCKOUT ON PARITY ERROR TEST*
01	BLANK
02	ADDR XXXXXX
03	PARITY ERR EXP (CMC/CSU ADDR)
04	PARITY ERR REC (CMC/CSU ADDR/NONE)
05	FORCE ZERO ON

The following three lines are added to the first display if write lockout is not working.

06	DATA EXP	7777 7777 7777 7777 7777
07	DATA REC	XXXX XXXX XXXX XXXX XXXX
08	WRITE LOCKOUT FAILED	

CPM

Loading

CPM (Central Memory Resident Test) runs under the control of CPC. The test requires three fully operational PPs and their associated channels to be able to run, plus one loading channel. LDR resides in PP0, MTR in PP1, and CPC in PP10. If the test is loading in auto mode, only the test mnemonic CPM need be entered. MTR is loaded automatically in auto mode. If auto mode is not selected, MTR must be loaded manually by entering the mnemonic MTR. CPM may be loaded before or after MTR. The test must run with the CEJ/MEJ switch in the disabled position. When starting and stopping the CPU, whether by keyboard command or by software, the B display must be selected so that the exchange is done with the last output package. All keyboard commands and displays are handled by CPC. The I display is used for all messages from CPM. After CPM and MTR have been loaded, the B and I displays should be selected before the test is given a go (hitting the spacebar). The test may be restarted by setting P=30B when the CPU is stopped. Test parameters are from RA+5 to RA+20B.

When CPM is initialized, the system identification bits are read and parameter word 20B is set for the appropriate model. Certain locations in the diagnostic are modified after the parameter stop is made to make the diagnostic compatible with the model, specifically the CDC CYBER 175.

This test does not check addresses 0 to 1777B in CM due to multiprogramming restrictions. This area is utilized by SMMs central memory resident tables. The test may be loaded in any area of memory above location 1777B with one restriction. The test may be loaded at location 2000B if no PP tests are running that require CM overlays. If PP tests that require overlays are running, the test should not be loaded below the overlay area.

Parameter Display

CPU STOPPED READY FOR PARAMETERS

To restart CPU after program stop, backspace and space.
To stop CPU, backspace.
To start CPU, space.

WARNING

MTR must be loaded prior to test execution. MTR is loaded automatically in auto mode or may be loaded manually at this time by entering the mnemonic MTR(CR).

When starting and stopping the CPU, the B display must be selected so that the exchange is done with the last output package.

The test must run with the CEJ/MEJ switch in the disabled position.

CM Parameters

3,4	Not used	
5	X XXX XXX XX1	Loop on failure
	X XXX XXX X1X	Stop on error
	X XXX XXX 1XX	Stop at end of section
	X XXX XX1 XXX	Stop at end of test
	X XXX X1X XXX	Repeat section
	X XXX 1XX XXX	Repeat test
	X XXX XXX XXX	Not referenced by this test
	X X1X XXX XXX	Repeat condition
	X 1XX XXX XXX	Stop at end of condition
	1 XXX XXX XXX	Abort error checking

6	Section Flags	
7	= 000...000	Use program supplied seed
	= XXX...XXX	Use XXX...XXX as seed
10	Bit 0 = 0	Bank mode
	Bit 0 = 1	Sequential addressing mode
11	= 000...XXXXXX	Upper limit
12	= 000...XXXXXX	Lower limit
13	= 000...UVW	Lower bank absolute
14	= 000...UVW	Upper bank absolute
15	= 000...XXXXXX	Number of write cycles
16	= 000...XXXXXX	Number of read cycles
17	= 000...XYYY	Delay count
20	= Bit 0 = 0	System is not a CDC CYBER 175.
	Bit 0 = 1	System is a CDC CYBER 175.
21	= Bit 0 = 0	Normal operation
	Bit 0 = 1	CSI mode

Running/Error Display

CDC CYBER 170 CPM

(SECTION TITLE)

SECTION	CONDITION	PASS
XX	XX	XXXX

(STOPPED) REPEATING (TEST/SEC/COND)

CSU X QUAD X CHIP X BANK X
CSU X QUAD X BANK X

QUAD X CHIP X BANK X
QUAD X BANK X

ADDRESS XXXXXX
EXP DATA XXXXXXXXXXXXXXXXXXXX
REC DATA XXXXXXXXXXXXXXXXXXXX
ADDRESS BIT BEING TESTED XX

SINGLE ERROR SYNDROME XXX ARRAY XX
DOUBLE ERROR SYNDROME XXX ARRAY XX
SUSPECTED MODULE XXX CHASSIS X

CMC PARITY ERROR ON CPU ADDRESS
CMC PARITY ERROR ON CPU DATA
CM PARITY ERROR ON CSU-0 ADDRESS
CM PARITY ERROR ON CSU-1 ADDRESS

CPU EXITED ON DATA INPUT PARITY ERROR

UPPER LIMIT EXCEEDED
LOWER LIMIT EXCEEDED

BREAKPOINT ERROR

ADDRESS XXXXXX CPU PORT ON READ
ADDRESS XXXXXX CPU PORT ON WRITE
ADDRESS XXXXXX CPU PORT ON RNI
ADDRESS XXXXXX CPU PORT ON ANY ACCESS

SECTION TITLE -	(ADDRESSING TEST	)
	(STANDARD PAT TEST	)
	(RANDOM PAT TEST	)
	(RANDOM ADDRESS TEST	)
	(DATA REFRESH TEST	)
	(BREAKPOINT TEST	)
STOPPED -	(STOPPED AT END OF TEST	)
	(STOPPED AT END OF SECTION	)
	(STOPPED AT END OF CONDITION	)
	(STOPPED ERROR DETECTED	)

CSI

CSI is run only after either CPM or CSP has been run in CSI mode and has stopped with the message DEAD START LOAD CSI.

CSI locates the error buffer created by CSP or CPM and displays a table of probable failures in descending order of probability. No operator entry is required other than the entry of a spacebar to start CSI.

CNF

CNF is a conflict test of central memory control to ensure that central memory control is capable of coordinating simultaneous access by any set of central storage users.

CNF operates under STM as a stand-alone test. It is loaded in the standard manner under SMM using the mnemonic CNF. The CEJ/MEJ switch must be in the ENABLED position, and the SCR should be cleared before calling the test.

Standard STM parameters apply through word 12. Parameter words 13 through 23 are as follows:

Word 13 Bit 0 = 0 All PPs operate at single speed
Bit 0 = 1 All PPs operate at double speed

Word 14 Bit 0 = 0 Disable ECS conflicts
Bit 0 = 1 Enable ECS conflicts

Word 15 Bit 0 = 0 Inhibit program overwrite check
Bit 0 = 1 Enable program overwrite check

Word 16 Quadrants of central memory to be used:

Bit 0 = 1 Use quad 0
Bit 1 = 1 Use quad 1, etc.

Words 17 through 20

Banks of CM to be tested in section 4 (bank overload test):

Bit 0 = 1 Test bank 0
Bit 1 = 1 Test bank 1, etc.

Word 21 Error exit mode selection:

Bit 0 = 1 Address range error mode
Bit 1 = 1 Infinite mode
Bit 2 = 1 Indefinite mode
Bit 3 = 1 Data parity error mode
Bit 4 = 1 CMC input error mode
Bit 5 = 1 Double SECDED error mode

Word 22 = 00XX

Display errors commencing at the XXth entry of the error buffer.

NOTE

Parameter word 22 is always reset to 0000 when a go is given after an error is displayed.

Word 23 Bit 0 = 0 Inhibit stop on SCR status monitor errors
Bit 0 = 1 Enable stop on SCR status monitor errors

PPU NUMBERING CHART

AUTO DDD DMP(LP) PC1	CH2 CHT IP1 PCM PM1 PMM PSP SSP	CH1 MAP PRW SCOPE DMP(DISP)	SCOPE Deadstart Dump	Physical Channel Numbering	Physical PPU Numbering
0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
10	10	8	8	10	10
11	11	9	9	11	11
				12	
				13	
				14 (RTC)	
				15 (INT. REG)	
12	20	10	A	20	0
13	21	11	B	21	1
14	22	12	C	22	2
15	23	13	D	23	3
16	24	14	E	24	4
17	25	15	F	25	5
20	26	16	G	26	6
21	27	17	H	27	7
22	30	18	I	30	10
23	31	19	J	31	11
				32	
				33	

REFERENCE GRID

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck of MNF	ENS	Stand-Alone	OVL	MLP	PSIO	STM
	Central Memory Tests														
CM6	6X00 CM test - more effective on 6600's	X	X			Y	N	N	N	N	Y	N	Y		
MCY	Modified M98 to run on 131K CYBER 70 machines		X			Y	N	N	N	N	Y	N	N		
MMX	Peripheral processor test of CM			X	X	Y	Y	N	Y	Y	Y	N	N	N	N
MM1	Test central memory from CPU	X	X			Y	N	N	N	N	Y	N	N		
MM2	Peripheral processor test of central memory	X	X	X	X	Y	Y	N	Y	Y	Y	N	N		
MM3	Same as MM1 but more rigorous and lengthy (CPU0+1)	X	X			Y	N	N	N	N	Y	N	N		
MM4	Central memory test that runs under auto	X	X			Y	N	Y	N	N	Y	N	Y		
MY1	Central memory test	X	X			Y	N	N	N	N	Y	N	Y		
M1A	32K equivalent of MM1	X	X			Y	N	N	N	N	Y	N	N		
M1B	32K equivalent of M1R	X	X			Y	N	N	N	N	Y	N	N		
M1C	49K or 98K memory test - a modification of M1R	X	X			Y	N	N	N	N	Y	N	N		
M1R	Same as MM1 with all the PPUs doing phased read of CM	X	X			Y	N	N	N	N	Y	N	N		
M2C	Version of MM2 modified to run on 49K or 98K machines	X	X			Y	Y	N	Y	N	Y	N	N		

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck of MNE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
M2U	Same as MM2 but for unphased memories only	X	X			Y	Y	N	Y	Y	Y	N	N		
M3A	Same as M3B and M3R but without PP reads	X	X			Y	N	N	N	N	Y	N	N		
M3B	Same as M3R but modified to run on 32K machine	X	X			Y	N	N	N	N	Y	N	N		
M3C	49K or 98K memory test - modified version of M3R	X	X			Y	N	N	N	N	Y	N	N		
M3R	CM test with all PPs doing phased block reads during the testing CYL	X	X			Y	N	N	N	N	Y	N	N		
M65	-32K, 65K, or 131K central memory test	X	X			Y	N	N	N	N	Y	N	N		
M98	Same as M65 but modified for 49K or 98K machine	X	X			Y	N	N	N	N	Y	N	N		
	System Control Routines														
CEL	Preload control program	X	X	X	X	OPT						N	N		
CPC	SMM central processor control (refer to Auto)	X	X	X	X	Y						Y	Y		
DSCL	Deadstart card loader	X	X	X	X	N									

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck of MNE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
LDR	SMM loader/monitor	X	X	X	X	Y			Y	N	Y	N	Y		
PT6	66X card loader	X	X	X	X										
CPMTR	SMM CPU monitor		X	X	X	X									
PS	PP system interface	X	X	X	X	OPT									
MTR	Status and control register monitor			X	X	Y					Y	Y			
STM	Stand-alone test manager			X	X						Y				
	Peripherial Processor Tests														
CED	Peripheral processor deadstart command test	X	X	X	X	N						N	N		
CHP	Modified CH1 for CY17X			X	X	OPT	Y		Y	Y	Y	N	N		
CHT	Channel test	X	X			Y	Y		Y	Y	Y	N	N		
CHX	CY17X channel test			X	X	N	Y	N	Y	Y	Y	N	N	N	N
CH1	Channel test	X	X			Y	Y		Y	Y	Y	N	N		
CH2	Channel test for 20 PPU systems - 6000/CY70	X	X			N	Y		Y	Y	Y	N	N		
IP1	Interprocessor test - 6000 instruction conflict test	X	X	X	X	N	Y		Y	Y	Y	N	N		

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck of MNE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
IRT	Interlock register test for CYBER 70		X			N	N	Y	N	N	N	Y	Y	N	
MAP	Central memory access priority test for 6X00	X	X			Y	Y	N	Y	Y	Y	N	N	N	
PCM	PPU command test-6600/6400/6411	X	X	X	X	Y	Y	N	Y	Y	Y	N	N	N	
PCX	PPU command test	X	X	X	X	N	Y	Y	Y	Y	Y	N	Y	N	
PC1	Peripheral processor command test	X	X	X	X	OPT	Y	N	Y	Y	Y	N	N	N	
PC2	CY17X peripheral processor command test			X	X	N	Y	N	Y	Y	Y	N	N	N	N
PMM	Peripheral processor memory test	X	X	X	X	N	Y	N	Y	Y	Y	N	N	N	
PMX	PP memory test for auto operation	X	X	X	X	Y	N	N	N	N	N	N	Y	N	
PM1	Peripheral processor memory test	X	X	X	X	N	Y	N	Y	Y	Y	N	N	N	
SSP	Super saturate pyramid test	X	X	X	X	Y	Y	N	Y	Y	Y	N	N	N	
	ECS Tests														
DDP	CYBER 70 distributive data path diagnostic	X	X	X	X	Y	N	Y	N	N	N	Y	Y	N	
ECM	ECS multiprogramming test for 6000/CYBER 70/CY17X	X	X	X	X	Y	N	N	N	N	N	N	Y	N	
ECS	Extended core storage test for 6000/CYBER 70	X	X			Y	N	N	N	N	Y	N	N	N	
ECX	Modified ECS test for CY17X			X	X	Y	N	N	N	N	Y	N	N	N	

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck of MNE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
	GRID Tests														
RGI	6X00/6671/241-1 remote GRID with remote interface to A201	X	X			Y	N	N	N	N	Y	Y	N	N	
RGT	6X00/6671/241-1 remote GRID test	X	X			Y	N	N	N	N	Y	Y	N	N	
	Service Routines														
CLK	Real-time display and timing clock for 6000 SMM	X	X	X	X	Y		Y				N	Y	N	
CMC	Central memory conflict program	X	X	X	X	Y	N	Y	N	N	Y	N	Y	N	
DDD	Deadstart dump (not multiprogrammable) dumps PPs and CM	X	X	X	X	N		N					N	N	
DMP	Multiprogrammable dump of PPs, CM, and dayfile	X	X	X	X	Y	N	Y	N	N	N	N	Y	N	
DLY	Clock delay (under AUTO only)		X			Y		N		Y		N	Y	N	
EXC	6400/6600 multiprocessing routine	X	X	X	X	Y		Y		N	N	N	Y	N	

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck of MNE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
LST	SMM tape catalog service routine (60X-65X)	X	X	X	X	Y				N	Y	N	Y	N	
PSM	Peripheral service multiprogrammable	X	X	X	X	Y	N	N	N	N	N	Y	N		
PSP/PSQ	Peripheral service (not multiprogrammable) PSQ for 3245 controller	X	X	X	X	Y	Y	N	Y	Y	Y	N	N	N	
PST	I/O service routine under SMM	X	X	X	X	Y	Y	N	Y	Y	Y	N	N	N	
PSX	3000 peripheral service routine-under AUTO/SCOPE	X	X	X	X	N	Y	Y	Y	Y	Y	N	Y	Y	
TD1	Tape to disk routine	X	X	X	X	N									
UTL	C170 utility routine CY17X			X	X	N		N		Y	Y	N	Y	N	
	Diagnostics														
CNF	Central storage conflict test			X	X	Y	N	N	N	N	Y	N	N	N	
CO1	CPU instruction stack				X	Y	N	N	N	N	Y	N	Y	N	N
CPM	Test central memory from the CPU			X	X	Y	N	N	N	N	Y	N	N	N	
CPX	CPU control				X	Y	N	N	N	N	Y	N	N	N	N
CSC	Central storage test from CPU			X	X	Y	N	N	N	N	Y	N	N	N	N
CS1	CSU module isolation routine			X	X	N	N	N	N	Y	Y	N	N	N	Y
CSP	Test central memory (MOS) from the peripheral processor			X	X	Y	N	N	N	Y	Y	N	N	N	Y

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck of MNE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
DAT	CYBER 175 floating divide				X	Y	N	N	N	N	Y	N	Y	N	N
FFZ	CY17X function parity test			X	X	Y	N	Y	N	N	Y	N	Y	N	N
IAS	CPU instruction stack				X	Y	N	N	N	N	Y	N	N	N	N
IW5	CPU instruction stack				X	Y	N	N	N	N	Y	N	N	N	N
PPM	Peripheral processor memory test			X	X	N	N	N	N	Y	Y	N	N	N	Y
SCD	CSC from PPS SECDED test			X	X	Y	N	N	N	Y	Y	N	N	N	Y
SCR	Status and control register test			X	X	N	N	N	N	Y	Y	N	N	N	Y
SK1	CPU instruction stack				X	Y	N	N	N	N	Y	N	Y	N	N
SK2	CPU instruction stack				X	Y	N	N	N	N	Y	N	Y	N	N
SK3	CPU instruction stack				X	Y	N	N	N	N	Y	N	N	N	N
TRC	Transmission path and parity network test (CMC from CPU)			X	X	Y	N	N	N	Y	Y	N	N	N	Y
TRP	Transmission path test (CSU from PPS)			X	X	Y	N	N	N	Y	Y	N	N	N	Y
MA5	CYBER 175 multiply unit test				X	Y	N	N	N	N	Y	N	Y	N	N

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck of MNE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
	CPU Command Tests														
ALS/ALX	Random instruction test (tests stack registers and scoreboard)	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
BD1/BDP	CY70/6X00 compare/move instruction test		2/3	X		Y	N	Y	N	N	N	N	Y	N	
BGK	30-bit instruction test	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
CMS/CMT	Random compare/move unit test for CY72/73		2/3	X		Y	N	N	N	N	Y	N	Y	N	
CTC	CPU portion of CT1 CPU command test	X	X	X	X	Y	N	N	N	N	Y	N	N	N	N
CT1	Fixed operand command test	X	X	X	X	Y	N	N	N	N	Y	N	N	N	
CT3	6000 random instruction test with CPU simulation	X	X	X		Y	N	N	N	N	Y	N	Y	N	
CT7	CYBER 175 command test (random) with simulation				X	Y	N	N	N	N	Y	N	Y	N	
CU1	Central processor command test	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
CU2	Central processor command test (binary only)	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
CU3	Central processor command test (binary only)	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
CU4	CYBER 175 command test				X	Y	N	N	N	N	Y	N	Y	N	
EJT	Exchange jump test - 6400/6500/6600, CY70	X	X			Y	Y	N	Y	Y	Y	N	N	N	
EJ1	Modified EJT for CY170			X	X	Y	Y	N	Y	Y	Y	N	N	N	
ERX	Error exit test	X	X	X	X	Y	N	Y	N	N	Y	Y	Y	N	

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck of MINE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
FDT	Floating divide test	X	X	X		Y	N	N	N	N	Y	N	Y	N	
FM1	Floating multiply test	X	X			Y	N	N	N	N	Y	N	Y	N	
FM2	Floating multiply test	X	X			Y	N	N	N	N	Y	N	Y	N	
FST	Random command test-fast version of RAN	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
IMC	6000/CY70 integer multiply test	X	X	X		Y	N	N	N	N	Y	N	Y	N	
IWS	6600 instruction stack test	X	X			Y	N	N	N	N	Y	N	Y	N	
LAT	Long add unit test	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
MAN	6X00/CY70 - CEJ/MEJ/MAN instruction test	X	X	X	X	Y	N	Y	N	N	N	Y	Y	N	
MXJ	6000/CY70 - monitor exchange jump (2610) and central exchange jump (013BJ+K)	X	X	X	X	Y	N	N	N	N	Y	N	N	N	
POP	Population counter test	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
RAN	Random number command test	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
RTJ	Return jump test	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
RX7	Random instruction test	X	X	X	X	Y	N	N	N	N	Y	N	Y	N	
STC	6600 instruction stack test 6600CY74					Y	N	N	N	N	Y	N	Y	N	
STK	Stack test 6600CY74					Y	N	N	N	N	Y	N	Y	N	
TOC	Third order conflict test - 6600/CY74 6600CY74					Y	N	N	N	N	Y	N	Y	N	

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck MNE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
	Magnetic Tape Tests														
ATC	67X controller test	X	X	X	X	Y	N	Y	N	N	Y	Y	Y	N	N
MMT	6X00/6681/3518-3528/657-859 magnetic tape test	X	X	X	X	Y	N	Y	N	N	Y	Y	Y	N	
MTA/MTB	67X tape unit test	X	X	X	X	Y	N	Y	N	N	N	Y	Y	N	N
MTT	3X2X/60X tape test (60X only)	X	X	X	X	Y	Y	Y	Y	Y	Y	Y	Y	N	
RGG	Record gap generation test	X	X			N	Y	Y	Y	Y	N	N	Y	Y	
TCT	6XXX/3X2X/604-607/657-659 tape compatibility test	X	X	X	X	N	N	Y	N	N	Y	N	Y	Y	
T5X	6000/CY70/CY170 65X tape test	X	X	X	X	Y	N	Y	N	N	N	Y	Y	N	
	Line Printer Tests														
FTP	580 fast train printer test	X	X	X	X	Y	N	Y	N	N	Y	Y	Y	N	
LP1	6X00/6681/3555/512 line printer test	X	X	X	X	Y	N	Y	N	N	Y	Y	Y	N	
PFC	580 programmable format control	X	X	X	X	N	N	Y	N	N	Y	Y	Y	N	N
	Card Reader/Card Punch Tests														
CP1	3446/3644-415 card punch test	X	X	X	X	N	Y	Y	Y	Y	Y	N	Y	N	
CR1	6X00/3649/3447/405 card reader test	X	X	X	X	N	Y	Y	Y	Y	Y	N	Y	N	

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck MINE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
	Buffer Controller Diagnostics														
BCX	Buffer controller command test	X	X	X	X	N	N	N	N	N	N	N	N		
BCY	844/66X controller memory test	X	X	X	X	Y	N	Y	N	N	Y	Y	Y	N	N
CDM	844 MTS coupler test	X	X	X	X	Y	N	Y	N	N	N	Y	N		
CID	Coupler test	X	X	X	X	Y	N	Y	N	N	N	Y	N		
FTD	FA205 coupler diagnostic	X	X	X	X	Y	N	Y	N	N	Y	Y	Y	N	N
LCC	Local communications controller	X	X	X	X	Y	N	Y	N	N	Y	Y	Y	N	N
MTC	Controller test	X	X	X	X	Y	N	Y	N	N	Y	Y	N		
MTS	66X tape test	X	X	X	X	Y	N	Y	N	N	Y	Y	N		
MY8	844/66X memory test	X	X	X	X	N	N	N	N	N	N	N	N		
MY9	844 memory test	X	X	X	X	N	N	N	N	N	N	N	N		
DTA	844 disk test	X	X	X	X	Y	N	Y	N	N	Y	Y	Y		
DTB	844 disk test	X	X	X	X	Y	N	Y	N	N	Y	Y	Y		
SAC	7077 coupler test	X	X	X	X	Y	N	Y	N	N	Y	Y	Y	N	N
	Display Tests														
DS1	6000/CYBER70/6602/6612/DD6 display alignment test	X	X	X	X	N	Y	Y	Y	Y	Y	N	Y		

Test	Description	6000	CY70	CY172/ CY173/174	CY175	CM	Deadstart Binary	PS	DSCL Binary Deck MNE	ENS	Stand-Alone	OVL	MLP	PSIO	STM
	Digital Communication Tests														
TT3	6X00/6676/103-A/103-B/ASR33 Teletype test	X	X	X	X	N	Y	Y	Y	Y	Y	N	Y		
TT5	6X00/6681/3266-3276/321 (8518 and 8519/ASR33 Teletype test	X	X			N	Y	Y	N	N	Y	N	Y		
	Remote Terminal Tests														
RT3	6X00/6673/6674/6675 data set controller test for 8230-8231 terminals	X	X	X	X	N	Y	Y	Y	Y	Y	N	Y		
RT5	6X00/6671 and TTY33 or TTY35	X	X	X	X	Y	N	Y	N	N	Y	Y	Y		
RT6	6X00/6671/201/200 user terminal	X	X			Y	N	Y	N	N	Y	Y	Y		
RTX	6X00/6681/3266/311/200 user terminal	X	X			Y	N	Y	N	N	Y	N	Y		
	Mass Storage Tests														
DF7/DF9	6X00/6681/3553-1/821-X or 841-X disk test	X	X	X	X	Y	N	Y	N	N	Y	Y	Y		

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